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A Variable Capacitor Made from Single Crystal Silicon Fracture Surface Pairs

by

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Abstract

Complementary and nano-smooth single-crystal-silicon surfaces have been fabricated by deliberately fracturing a weakened portion of a larger structure whose flexural mechanism refines and concentrates an externally applied load to a notched specimen region pre-fracture and acts as a precision bearing post-fracture. When material is not ejected, crystalline silicon's extreme brittleness at room temperature results in complementary fracture surfaces; "closed" gaps of 20-30 nanometers are typical. Lithographic, focused ion beam, and anisotropically etched notches as well as crystal orientation and specimen thickness were studied, and a method was developed for fabricating smooth surfaces perpendicular to the wafer plane: 10 micrometer square specimens oriented with the (110) plane are fully notched by anisotropic etching (KOH) and fractured within a structure optimized to apply pure tension.

Prototype MEMS variable capacitors employing fracture surfaces as separable parallel plates have been developed. The advantage of fracture surfaces over etched surfaces is their exceptional flatness or complementarity, which allow them to very closely approach each other prior to contact. For a parallel-plate capacitor, a small minimum separation disproportionately improves dynamic range because capacitance scales with the inverse of separation. To take utmost advantage of the surfaces' qualities, unstable pull-in must be avoided. Modelling of the three-way force balance between the structure's compliance, the capacitive force between the fracture surfaces, and the zipping electrostatic actuator demonstrates the system is stable when the actuator is working against the spring force and not the capacitive force. The structure and the capacitor are tuned to ensure system stability to nanometer scale separations.

During fabrication of the variable capacitor, it was discovered that high temperature processing associated with the thermal oxidation necessary for the actuators blunted the anisotropically etched notches. This blunting occurred even when the notches were covered with a nitride diffusion barrier, and was likely due to diffusional smoothing. Blunt notches produced material ejecting fractures with non-functional surfaces, but since material ejection is characteristic of higher stress fractures, it may

be useful for toughening anisotropically etched structures. The blunting problem was overcome by masking the notch etch with thermal oxide after all high temperature processing was complete.

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Nomenclature

Δ	Maximum stroke of the zipper (μm)
δ	A simplification, defined in Equation 4.8
ϵ_r	Dielectric constant of the zipper dielectric, 3.8 for silicon dioxide
ϵ_w	Dielectric constant of water, 78.5
ϵ_0	Permittivity of free space, $8.854 \cdot 10^{-12} \frac{\mathrm{F}}{\mathrm{m}}$
η	A simplification, defined in Equation 4.41
κ	Debye constant $(\frac{1}{m})$
λ	X-ray wavelength for EDX calculations (m)
λ_D	Debye length (m)
j	$\sqrt{-1}$
K	Stiffness matrix for two-node model $(\frac{mN}{\mu m})$
M	Mass matrix for two-node model (mg)
ω	Excitation frequency for the variable capacitor device $(\frac{\mathrm{radians}}{\mathrm{s}})$
ϕ	A simplification, defined in Equation 4.38
ψ	A simplification, defined in Equation 4.40
σ_m	Specimen moment stress (MPa)

σ_t	Specimen tensile stress (MPa)
θ	A simplification, defined in Equation 4.39
$\tilde{\omega}_n$	Linearized natural frequency $\left(\frac{\text{rad}}{\text{s}}\right)$
ζ	Generalized coordinate
A	Area of one capacitor plate (μm^2)
A_s	Specimen cross sectional area (m^2)
B	A simplification, defined in Equation 4.4
b	Thickness of the zipper, typically also the SOI device layer thickness (μm)
C	A simplification, defined in Equation 4.7
c	Distance from the neutral axis (m)
C_2	Reference capacitor in capacitance measurement circuit (pF)
C_3	Parasitic capacitance in capacitance measurement circuit (pF)
C_g	Variable capacitor in capacitance measurement circuit (pF)
C_{device}	Capacitance of the device(F)
C_{ox}	Capacitance of the native oxide on the fracture surfaces (F)
C_{par}	Parasitic capacitance (F)
c_p	speed of light, 299,792,458 $\frac{\text{m}}{\text{s}}$
C_{var}	Variable capacitance between the fracture surfaces (F)
d	Separation of the fracture surfaces, Casimir force measurement (m)
E	Energy of K-series X-ray transitions
e	Voltage vector for modelling the variable capacitor device (V)

F	Faraday's constant, 96,485 $\frac{\text{C}}{\text{mol}}$
F_c	Capacitive force (mN)
F_k	Spring force for single node model (mN)
F_p	Preload force (mN)
F_r	Reaction force (MN)
F_z	Zipper force (mN)
F_{k_t}	Tether spring force
$F_{k_{sg}}$	Specimen stage spring force
$F_{k_{zg}}$	Input stage spring force
$F_{residual}$	A measure of the importance of secondary forces
$G_{external}$	Input impedance matrix for modelling the variable capacitor device (Ω^{-1})
$G_{internal}$	Conductance matrix for modelling the variable capacitor device (Ω^{-1})
h	Height of the zipper beam (μm)
h_0	Thickness of the zipper dielectric (μm)
h_p	Plank's constant, $4.136 \cdot 10^{-15}$ eV sec
I	Ionic strength (Molar)
I_{xx}	Second moment of inertia about the x-axis (m^4)
k	Spring constant for single node model $\left(\frac{\text{mN}}{\mu\text{m}}\right)$
k_t	Tether spring constant $\left(\frac{\text{mN}}{\mu\text{m}}\right)$
k_{zg}	Input stage spring constant $\left(\frac{\text{mN}}{\mu\text{m}}\right)$
k_z	Zipper connection spring constant $\left(\frac{\text{mN}}{\mu\text{m}}\right)$

m	Mass
m_1	Mass at Node I for the two-node model (mg)
m_2	Mass at Node II for the two-node model (mg)
M_r	Reaction moment (MN-m)
$M_{residual}$	A measure of the importance of secondary moments
N	Number of points in sample
P	Capacitance matrix for modelling the variable capacitor device (F)
Q	Zipper constant, $2.72 \cdot 10^{-6}$, derived from FEA
R	Ideal gas constant, 8.31 $\frac{\text{J}}{\text{K}\cdot\text{mol}}$
R_q	RMS roughness (nm)
R_{sk}	Skew
T	Temperature of the dielectric (K)
t_{ox}	Dielectric (oxide) thickness (m)
t_{var}	Capacitor plate separation (m)
v	External voltage vector for modelling the variable capacitor device (V)
V_c	Voltage across the capacitor (V)
V_z	Voltage across the zipper (V)
V_d	Capacitance divider voltage in capacitance measurement circuit (V)
V_{in}	Excitation voltage for capacitance measurement circuit (V)
V_{min}	Actuator voltage for the variable capacitor at which the minimum stable gap x_{min} is achieved (V)

V_{out}	Output voltage of capacitance measurement circuit (V)
x	Displacement for single node model (μm)
x_0	Equilibrium displacement of the single node model(μm)
x_1	Node I displacement (μm)
x_2	Node II displacement (μm)
x_{10}	Equilibrium displacement of Node I in the two-node model (μm)
x_{1p}	Perturbation from equilibrium of Node I in the two-node model (μm)
x_{20}	Equilibrium displacement of Node II in the two-node model (μm)
x_{2p}	Perturbation from equilibrium of Node II in the two-node model (μm)
x_{max}	Maximum specimen displacement in the variable capacitor device (nm)
x_{min}	Minimum stable separation of the surfaces in the variable capacitor device (nm)
z	Zipper displacement (μm)
z_i	Height of each point in the sample (nm)

Chapter 1

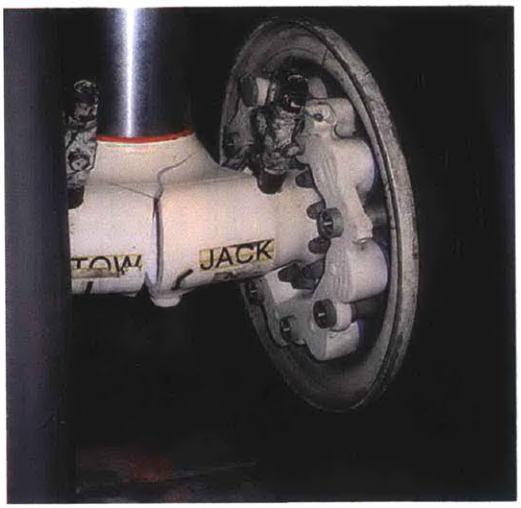
Introduction

Can fracture be useful? Or is it merely, as the National Bureau of Standards concluded in 1983, a phenomenon that costs the United States economy $119 billion per year (with 1978 as the basis year) [118].

Fracture is typically seen as a problem to be avoided, but in the images of Humpty Dumpty and the cracked aircraft main landing gear in Figure 1-1, the kernel of how fracture can be put to good use can also be seen: both fractures are brittle and have left behind complementary surfaces.

Single crystal silicon is an exceptionally brittle material [113], and its crystalline nature facilitates the creation of nano-smooth surfaces. As a material at the heart of the semiconductor industry, the tools and processes for microfabricating structures within it are highly developed. The aim of this thesis is to develop a process for the fabrication of pairs of precision silicon surfaces embedded within a supporting compliant mechanism and a Micro Electro-Mechanical System (MEMS) that employs such surfaces as the separable plates of a variable capacitor. Instruments based on the variable capacitor, which can precisely control the separation of the of the two fracture surfaces to create nanometer scale gaps, will complement devices like the Atomic Force Microscope (AFM), Scanning Tunneling Microscope (STM), and the Mechanically Controlled Break (MCB) junction [99], which rely on precise control of a pair of points or of a point and a plane. This thesis explores the utility of an equivalent level of control over a pair of planes [128], possible applications for which

(a) Humpty Dumpty posing with all the king's horses and all the king's men after his great fall.



(b) P-3 main landing gear. The crack was discovered during pre-flight inspection. [59]

Figure 1-1: A pair of images illustrating the context in which fracture is typically seen, as well as the complementary surfaces which could be useful for instrument design.

include variable capacitors, variable flow microvalves, impedance spectroscopy [47], and as an instrument for studying the physics of small gaps.

The fundamental contributions include the development of a process and specialized mechanism for the fracture fabrication of nano-smooth and complementary surfaces, the design of a variable capacitor employing fracture surfaces as its separable plates, and the fabrication of prototype variable capacitors with integrated actuators.

Figure 1-2(a) is a schematic of a fracture process development device. The process and this device will be described in detail in Chapter 2, but in brief: The folded-leg flexure concentrates an externally applied load at the specimen, where the fracture occurs. Post-fracture, the flexure supports one of the fracture surfaces and acts as a bearing to guide its motion so the two sides can be re-joined to form a complementary seal.

In Figure 1-2(b) is a micrograph of a prototype variable capacitor (Chapters 4 and 5). As in the process development device, a flexure concentrates an externally applied stress to induce fracture and acts as a bearing post-fracture. An integrated actuator controls the separation of the surfaces to vary the device's capacitance. In

these devices, the fracture does not result in two different pieces of material. The flexure in which the surfaces are imbedded remains intact to guide their separation. The surfaces, whether complementary or nano-smooth, are used together to create nanometer-scale gaps.

1.1 Prior Art

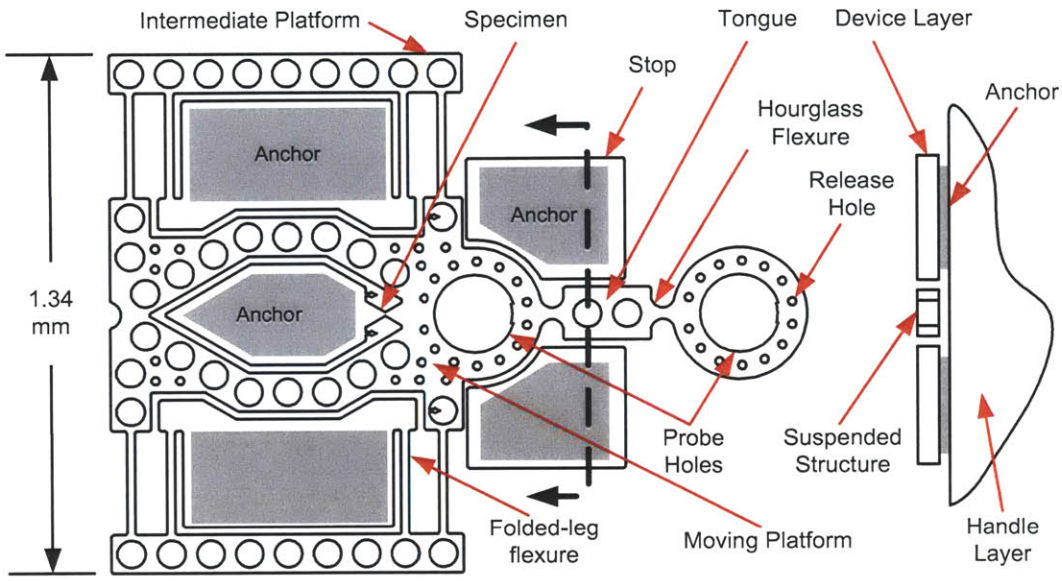
Existing technologies similar to the fracture fabrication of silicon surfaces presented in this thesis are discussed in the following sections. A brief description of each technology is followed by a summary of how it differs from the work of this thesis.

1.1.1 The Nanogate: Nanoscale Flow Control

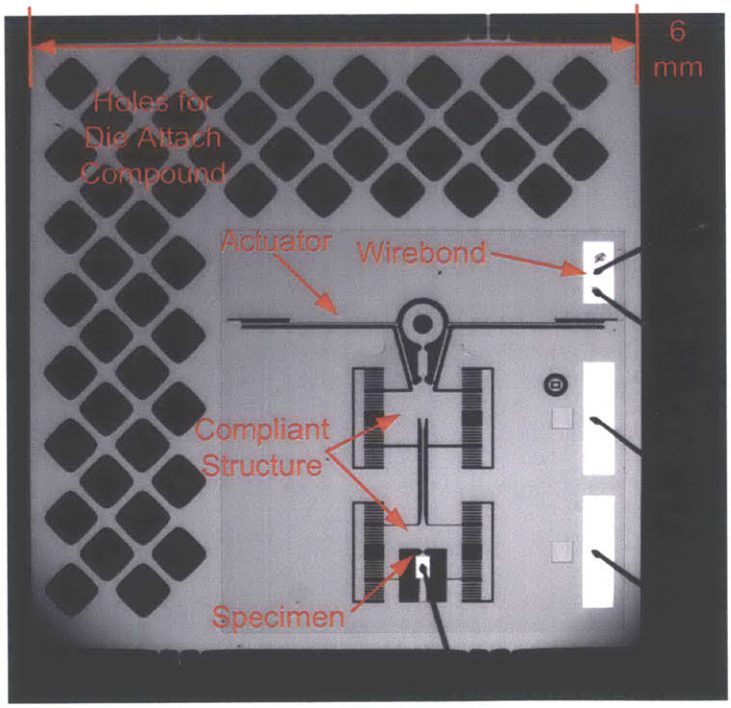
The Nanogate [143, 144], a device for nanoscale flow control, is depicted schematically in Figure 1-3. It is fabricated by etching the structure of revolution shown into a silicon wafer and then anodically bonding the silicon wafer to a pyrex wafer with a patterned gold surface. The gold on the pyrex wafer surface beneath the valve land prevents the two wafers from bonding there. Instead, the silicon hot embosses the gold covered pyrex to produce a gold surface that complements defects in the polished silicon land; the two surfaces seal exceptionally well.

Once fabrication is complete, the outer rim of the device is displaced downwards to actuate the valve. The flexible fulcrum, which unlike the land, is bonded to the pyrex wafer, converts large displacements at the rim to small displacements at the valve land, enabling the valve to be opened in 0.2 nm steps to a maximum separation of 1 μm without stiction in normal, non-dry air. The quality of the seal between the valve land and the embossed gold produces a minimum "closed," helium flow of $10^{-7}\ \frac{\text{atm}\cdot\text{cc}}{\text{s}}$ from a 6 psi drop into vacuum, a flow resolution of $10^{-9}\ \frac{\text{atm}\cdot\text{cc}}{\text{s}}$, and maximum flow of at least $10^{-3}\ \frac{\text{atm}\cdot\text{cc}}{\text{s}}$. Because of these exceptional flow control properties, the device is under evaluation by the National Institutes of Standards and Technology (NIST) as a transfer standard.

The differences between the Nanogate and the fracture derived devices in this

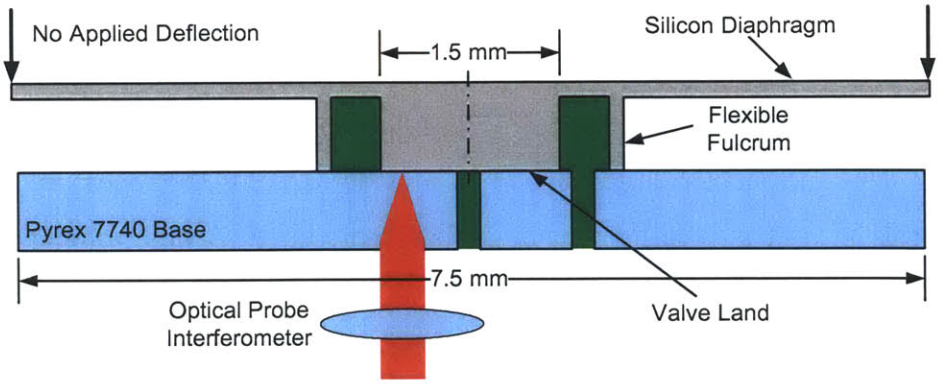


(a) A fracture process development device. Pre-fracture, the flexure concentrates stress at the specimen, and guides the separation of the surfaces post-fracture.

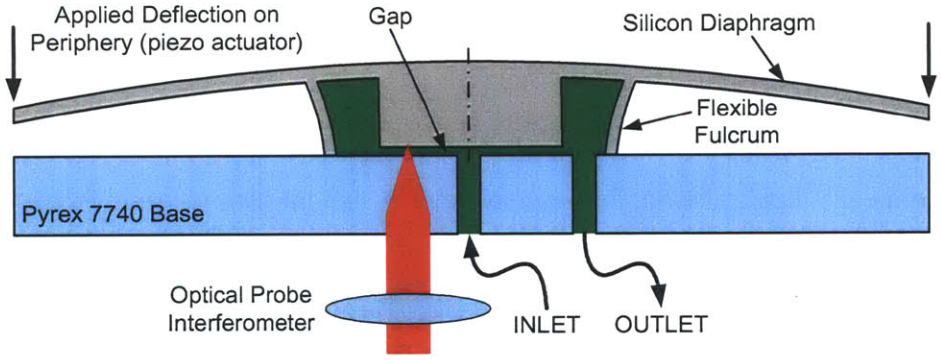


(b) A prototype variable capacitor device. The flexure serves a similar role as in the process development device, but also features an integrated actuator to control the surfaces' separation.

Figure 1-2: Fracture devices



(a) Closed Nanogate



(b) Open Nanogate

Figure 1-3: Schematic of the Nanogate in both closed and open configurations after [143]. Note how large deflections at the periphery are converted to small deflections at the valve land.

thesis arise primarily from the different surface creation methods. The Nanogate's reliance on hot embossing during the anodic bonding step precludes its use at high temperatures where the gold (or other metal) would soften or melt. Fractured surfaces are also less likely to be contaminated, since they are created from previously unexposed material.

1.1.2 Manufacturing Connecting Rods, Ball Races, etc.

The patents of Baude [11], Pierce [115], and Parks [112] employ fracture in a manufacturing and assembly processes for mating parts that are subsequently re-assembled on shafts. Unlike the fracture process that is the subject of this thesis, the intention is not to control the separation of the surfaces, but rather to achieve precision mating;

the part is fractured and then re-assembled once (Figure 1-4). Another difference is that the devices considered in this thesis are not divided into two parts. The fracture occurs within a structure that is never fully separated. Still another difference is scale. These inventions are intended to provide micron-scale repeatability. The goal of this project is to achieve nano-scale repeatability. A final difference is the potential to create perfectly flat surfaces. These inventions anticipate (even rely on) the formation of a rough, jagged fracture surface. That is a possibility with silicon, but an atomically smooth fracture surface is also a potential outcome.

1.1.3 Surface Force Apparatus

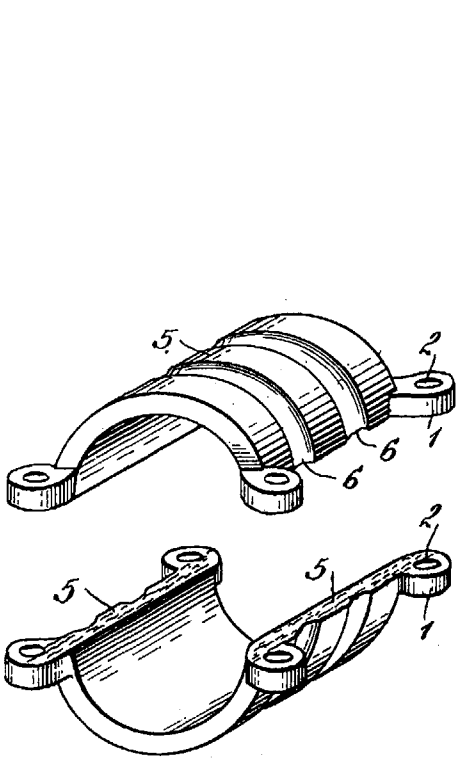
In a Surface Force Apparatus (SFA) (Figure 1-5), two crossed semi-cylinders covered with atomically flat mica are brought to within nanometers of each other to study the properties of fluids in small gaps [64, 61] or Van der Waals forces [133, 60, 62].

The fracture devices discussed in this thesis are fabricated in a different manner from an SFA; the mica surfaces in a SFA are cleaved, but not from each other. Furthermore, sensors and actuators that must be "bolted-on" to the SFA, may readily be integrated within a MEMS device.

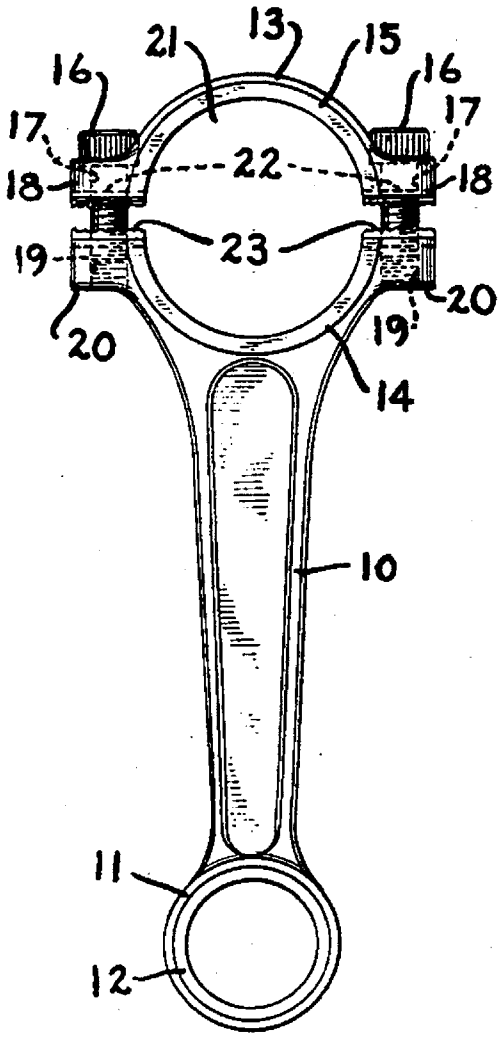
Atomically flat mica is also often used by itself as a substrate for AFM studies and occasionally as a template for the creation of ultraflat gold surfaces [53]. Such applications are quite different from the devices in this thesis in that only one surface is used.

1.1.4 Mechanically Controllable Break Junctions

Mechanically controlled break junctions [103, 114, 100] are the existing technology most similar to the the fracture devices described in this thesis. To create a MCB junction, a thin, brittle filament or whisker is epoxied to an elastic substrate, often a glass slide. The filament is mechanically notched (typically with a razor blade). For the resulting pair of surfaces to separate linearly, it is important the notch be equidistant from the two spots of epoxy fixing the filament to the substrate. The



(a) The two halves of a ball race, from Figure 2 of [115]. Note the fracture surfaces, 5, and the ball paths, 6. The patent is intended to join the paths without any disruption of their surface.



(b) A connecting rod, machined as one piece, is fractured and then assembled onto the crankshaft using the asperities on surfaces 22 and 23 to locate the two pieces, from [112].

Figure 1-4: Fracture surfaces employed as mating surfaces for precision assembly.

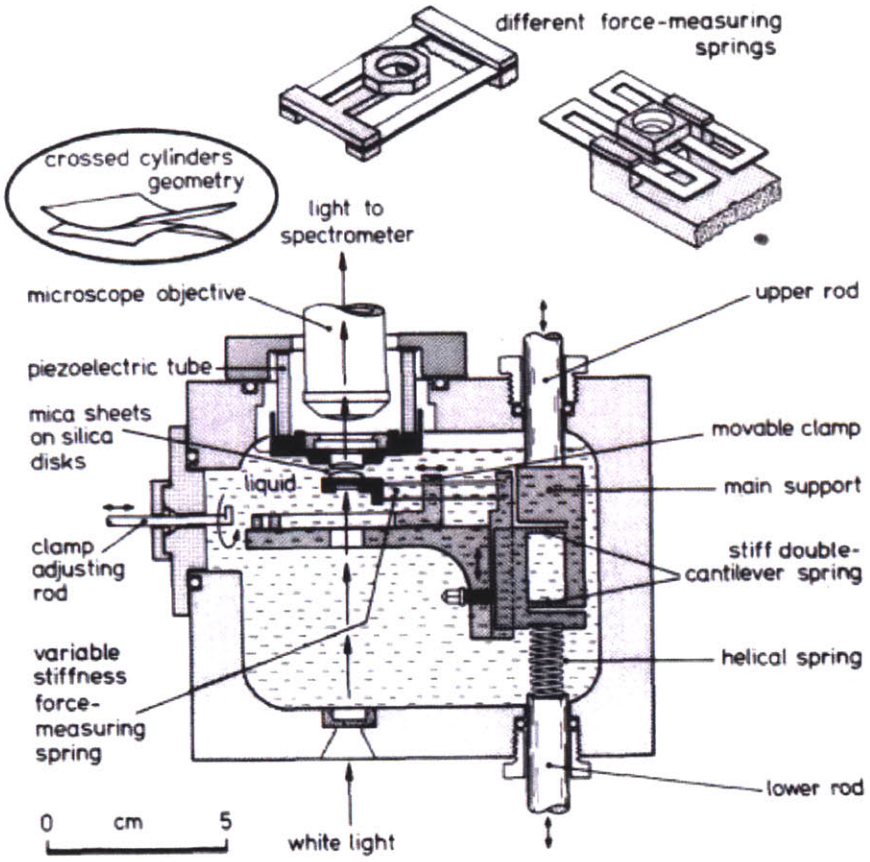


Figure 1-5: Surface Force Apparatus, from [63].

substrate (and filament) are then bent. The filament is on the outermost ligament of the assembly such that it encounters more strain than the substrate (Figure 1-6). When the filament breaks, two electrodes are created. The distance between these electrodes is controlled by bending the substrate. This apparatus is most commonly employed for various electron tunnelling experiments.

The conventional MCB junction fabrication process is quite different from the microfabrication processes for the devices in this thesis. The MCB junction process also makes it difficult to integrate other sensors. Most commonly, this manifests itself in the difficulty of independently determining the distance between the electrodes [70].

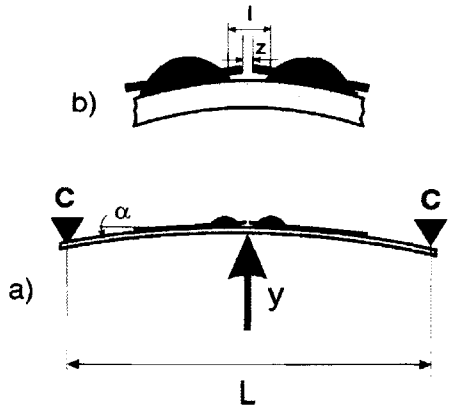


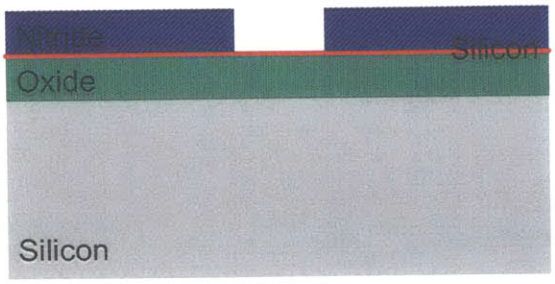
Figure 1-6: Schematic of a mechanically controllable break junction (a) with a detail view of the junction region (b), from [76]. The glass slide on which the filament is mounted is simply supported at points C and displaced at Y to control the distance z between the fracture faces of the filament.

1.1.5 SOI Cleaving Processes

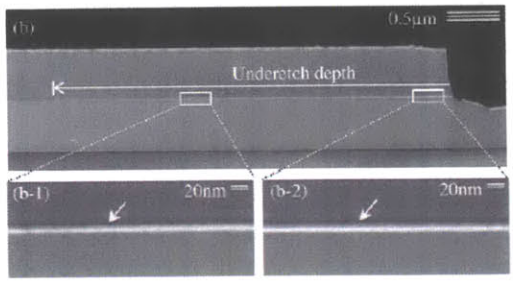
There is a superficial similarity between the fracture fabrication process in this thesis and various processes, e.g. Smart-Cut®, for creating Silicon On Insulator (SOI) wafers [32, p. 50]. In the SOI processes, a layer of silicon is cleaved (typically following an ion implantation [30]) from a donor substrate. This is different from the processes discussed here in many ways, chief among which are that the two pieces are completely separated and that the two fracture surfaces are not intended to be (and cannot be without great difficulty) used together.

1.1.6 Dicing Processes

There is also a superficial resemblance between the fracture fabrication process in this thesis and various processes used to dice wafers prior to packaging. The "Integrated Partial Sawing Process" of Mignardi and Alfaro [96] is a good example. Rather than cutting all the way through the wafer to be diced, only a partial cut is made. The wafer is then broken along these cleave lines. Another cleaving process [102] works on scribed wafers and employs a custom built fixture. These process are not intended for the fabrication of surfaces, but for the separation of pieces from a single crystal. Once fractured, the pieces are separated and cannot be matched back up.



(a) Fabrication cross section. Note the relative thickness of the sputtered silicon layer



(b) Cross sectional TEM images after a 3 nm film of silicon has been etched with XeF_2. From [48]

Figure 1-7: Sections illustrating the use of gas etching to create small gaps.

1.1.7 Gas etching

A paper by Hamaguchi et. al. [48] describes the fabrication of 3 nm gaps by the etching of a sacrificial silicon film with XeF_2. In this process (Figure 1-7(a)), a thermal oxide is grown on the wafer surface, a sacrificial layer of silicon is sputter deposited, and then a film of silicon nitride is deposited. After the nitride film is patterned with a series of holes, the wafer is exposed to XeF_2. The gas etches the the silicon exposed at the bottom of the holes and then etches laterally, undercutting the nitride (Figure 1-7(b)).

The size of the gap created by the process is determined by the thickness of the sacrificial layer. This is a big advantage considering the substantial investment in ultra thin film deposition that has been made by the semiconductor industry. The minimum achievable gap size is therefore determined by the size of the etching species. Significantly, it is substantially more difficult to deposit appropriate thin films normal to the wafer plane, limiting application of this technique to the creation of in-plane surfaces.

1.1.8 Thermal Cutting

Thermal cutting processes [106, 85, 138] employ laser heating to propagate a crack. The laser locally heats the substrate, creating a zone of compressive stress with a surrounding area of tensile stress (Figure 1-8). A crack tip within the area of tensile

stress advances. As the laser is scanned across the surface, the crack follows.

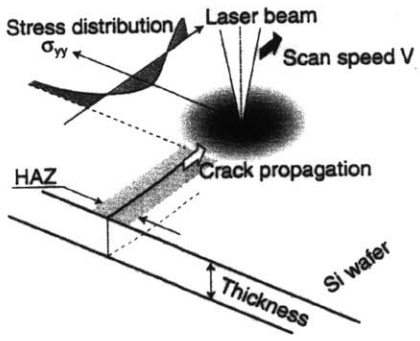


Figure 1-8: Thermal cutting concept from [138]. Laser heating creates compressive stress at the spot and an area of tensile stress around it.

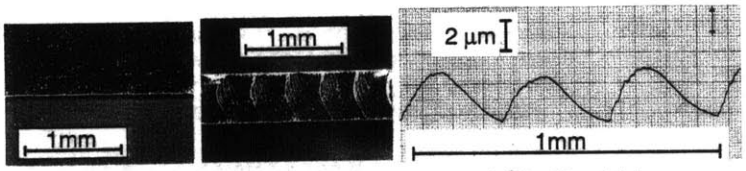
Thermal cutting is a potentially complementary process to the fracture process described in this thesis. Relatively smooth thermally cut surfaces have been demonstrated (Figure 1-9), and as the cracking is still brittle in nature, one would expect the resulting surfaces to be complementary. Thermal cutting is a serial process, but could be readily integrated with a MEMS process, which may even be useful for the creation of the necessary pre-cracks. A great deal of work remains to be done to optimize the process' many parameters to improve surface roughness, minimize the heat affected zone, and maximize throughput.

1.2 Applications

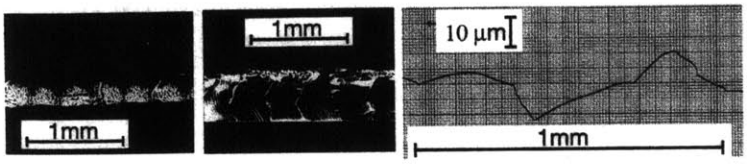
Concepts for several different types of devices based on the unique qualities of the fracture fabricated surfaces described in this thesis are outlined in this section.

1.2.1 Microfluidic Variable Flow Valve

A concept variable flow microvalve is illustrated in Figure 1-10, where the proportions of the device have been exaggerated for clarity. The fracture surfaces are embedded in a compliant structure for support. An actuator controls the separation of the surfaces, and microchannels transmit the fluid to the gap between the fracture surfaces. As



(a) Work surface (b)Fracture surface (c)Profile of (b)
Figure 6: Silicon wafer cleaved with Q=215 W (V=3.33mm/s, τ=2ms).



(a) Work surface (b)Fracture surface (c)Profile of (b)
Figure 7: Silicon wafer cleaved with Q=449 W (V=3.33mm/s, τ=2ms).

Figure 1-9: A pair of figures from [138] showing the results from different process parameters. Q is the laser power, V is the scan speed, and τ is the laser pulse duration.

with the Nanogate and [41], the flow is controlled by varying the separation of the surfaces to create a variable orifice.

The microchannels are fabricated by an Empty Space in Silicon (ESS) technique in which lines of silicon pits are covered over by defect-free single crystal silicon and coalesce during an anneal in a hydrogen atmosphere [123] (Figure 1-11). The defect-free nature of the silicon atop the "pipes" should prevent their integration with the fabrication process from interfering with the formation of the fracture surfaces. The "Hole-in-the-Wall" process [43] is less attractive than the ESS process because it would require process post-fracture and because it cannot be simultaneously used to make the necessary microchannels. This concept features three channels, two inlets and one outlet, with the output and inlet-2 microchannels fabricated within the beams of the folded leg flexure. Flow from the inlet channels is regulated by the variable orifice formed by the fracture faces (Figure 1-12). For a variable flow valve, only one inlet channel is required. Two have been shown here to suggest the possibility of mixing two different substances in the small space between the fracture surfaces. A pyrex cover (not shown in the figure) encloses the device. The large dead volumes associated with such an enclosure are naturally a concern, but would at this time

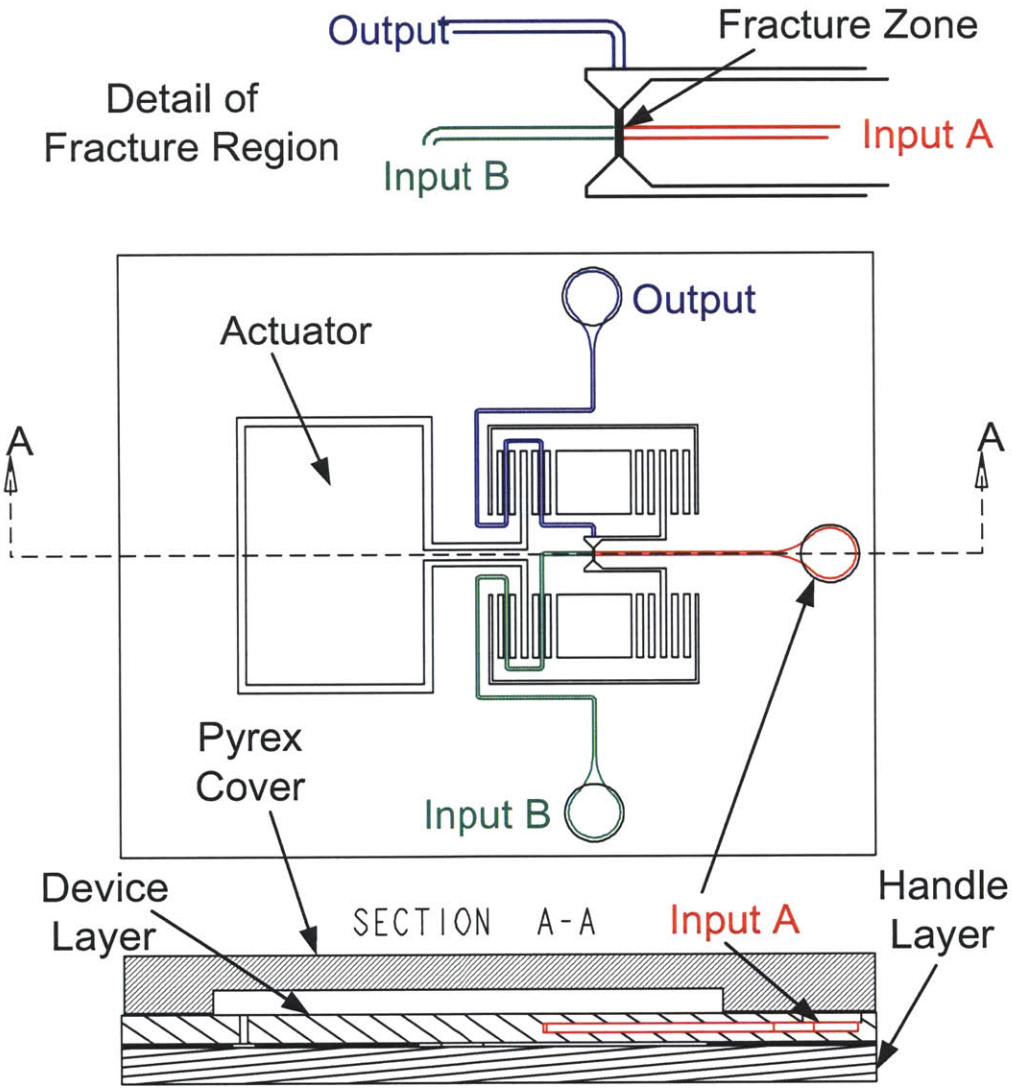
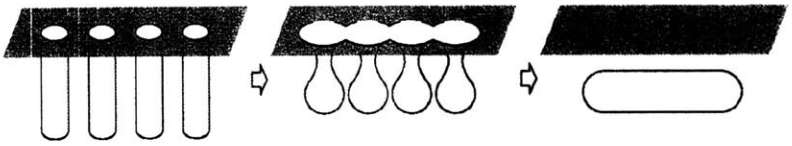
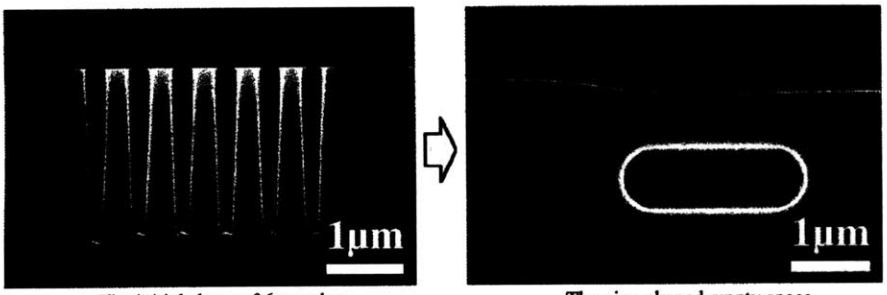


Figure 1-10: Variable flow microvalve concept. For clarity, the proportions of the device have been exaggerated.

likely be overwhelmed by the volumes associated with other ancillary hardware such as tubing and fittings.



(a) "Pipe-shaped empty space can be formed by combining the spherical empty spaces at the bottom of each trench."



(b) "SEM images showing the formation of a pipe-shaped empty space. ([left]) 6 trenches were arranged in a rc w. ([right]) The pipe-shaped empty space were formed by the combination of the spherical empty spaces formed at the bottom of 6 trenches, due to the annealing at 1100°C."

Figure 1-11: ESS illustrations and SEM images from [123].

Mating complimentary fracture surfaces are sufficient for the valve. The asperities on each surface combine to create a labyrinthine seal. Perfectly smooth, planar surfaces would be more similar to the Nanogate's surfaces and should work as well, but are more difficult to create, though they have the advantage of being less sensitive to imperfections in the flexure's guidance.

1.2.2 Casimir Force Measurement

The Casimir force [27] is an attraction between two neutral objects originating from deformations in the vacuum caused by boundary conditions imposed by the objects. For conducting parallel plates, the attraction is described by the equation [18]

$$F_{casimir} = \frac{A_s \pi h_p c_p}{480 d^4}, \tag{1.1}$$

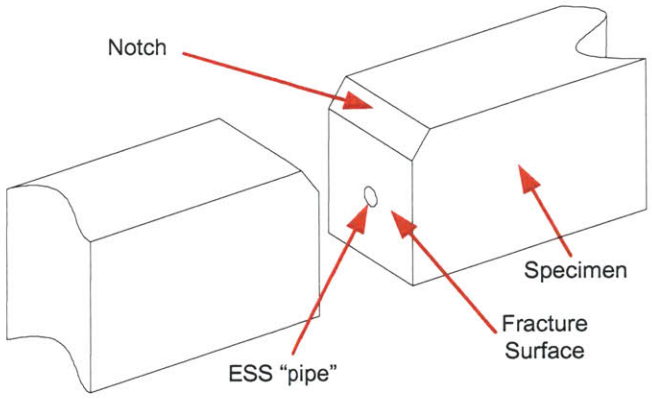


Figure 1-12: A close-up, oblique view of concept microvalve. The valve is shown wide-open for clarity. Fluid flows from the microchannel and through the variable orifice formed by the narrow separation of the fracture surfaces.

where, A_s is the area of the plates, h_p is Planck's constant, c_p is the speed of light, and d is the separation of the plates. Additional terms can be added to account for other effects such as the surface finish of the plates, but perfectly smooth parallel fracture surfaces would produce the cleanest results.

The fracture surfaces' ability to closely approach each other without touching makes them a good candidate for integration into a device for measuring Casimir forces. The Casimir force between parallel plates has not yet been measured at distances below 300 nm [26]; the difficulties associated with bringing parallel plates into close proximity has made the less useful [18] but more readily implemented sphere and plane configuration [140] much more frequently studied. Micrographs of re-sealed fracture devices indicate they can approach each other considerably closer than 300 nm (Figures 2-20 and 2-27).

The challenges of constructing such a device are the detection of forces at the nano-newton level and proper control of the separation of the two fracture surfaces. Not only are the forces to be measured small, but the device must be deliberately designed so that the Casimir force can be distinguished from other forces that may be present, e.g. electrostatic, spring, gravitational, etc.

1.2.3 Variable Capacitor

Chapters 4 and 5 describe the design and fabrication of a variable capacitor. Applications for such a device include Radio Frequency (RF) MEMS [150] and, with the addition of microfluidic channels, dielectric spectroscopy [47].

For a variable capacitor, the fracture surfaces are used as parallel plates whose separation is controlled with an integrated actuator. Fracture fabricated surfaces have an advantage over etched surfaces because they can approach each other to nanometer levels without touching. This close-approach capability increases the maximum capacitance of the device and thus its dynamic range. One of the principal challenges is minimizing the stable separation of the surfaces in the presence of a strong pull-in force. Another is the minimization of the parasitic capacitance.

As with the microvalve, both complementary and nano-smooth surfaces may be used in a variable capacitor. The smooth planar surfaces are advantageous because of their reduced sensitivity to guidance errors as well as the absence of the electrical field concentrating asperities present on the complementary surfaces. Such asperities are a concern because they enhance tunnelling, which would not be present in an ideal capacitor.

The variable capacitor described in Chapters 4 and 5 is not particularly competitive for RF-MEMS applications (Table 1.1). It's tuning ratio,

$$\text{Tuning Ratio} = \frac{C_{max}}{C_{min}}, \tag{1.2}$$

is not very competitive with other devices in the literature. The relatively low tuning ratio is largely a consequence of the devices's large parasitic capacitance. Potential avenues for the reduction of the parasitics will be discussed in the final chapter.

Though proper fluid interconnects would have to be added, the variable capacitor described in this thesis is potentially much more at home as an instrument for dielectric spectroscopy. Conventional dielectric spectroscopy is Debye length limited; the signal from the sample is masked by a pair of double layers that build up at each electrode (Figure 1-13). By operating at a gap of the same order as the Debye length,

	Actuation Voltage (V)	Minimum Capacitance (pF)	Maximum Capacitance (pF)	Tuning Ratio
Nguyen, Hah, et. al. [108]	40	0.27	8.60	31.9
Borwick, Stupar, et. al. [15]	8	1.40	11.9	8.4
Xiao, Peng, et. al. [149]	75	0.95	5.55	5.9
Zou, Liu & Schutt-Aine [152]	20	0.03	0.08	2.6
Hung & Senturia [56]	40	0.55	1.00	1.8
Fracture Capacitor	200	0.81	1.16	1.4
Young & Boser [151]	5.5	2.11	2.46	1.2
Seok, Choi & Chun [125]	8	1.40	1.54	1.1

Table 1.1: Performance of MEMS variable capacitors, courtesy of Xue'en Yang. The expected performance parameters of the capacitor described in this thesis is in the "Fracture Capacitor" row.

however, a fracture based device would measure the impedances of the sample and the double layer in parallel rather than in series, greatly improving sensitivity.

The Debye length is calculated with the equation [57]

$$\lambda_D = \frac{1}{\kappa} = \sqrt{\frac{\epsilon_0 \epsilon_w RT}{2000 I F^2}}, \tag{1.3}$$

where ϵ_0 is the permittivity of free space, $8.854 \cdot 10^{-12}\ \frac{\mathrm{F}}{\mathrm{m}}$, ϵ_w is the dielectric constant of water, 78.5, R is ideal gas constant, $8.31\ \frac{\mathrm{J}}{\mathrm{K \cdot mol}}$, T is the temperature in Kelvin, F is Faraday's constant, $96{,}485\ \frac{\mathrm{C}}{\mathrm{mol}}$, and I is the ionic strength of the salt in Molar (moles per liter of water). Equation 1.3 is plotted in Figure 1-14 for $T = 25°\mathrm{C}$. For systems of most interest in colloid science, $\frac{1}{\kappa}$ ranges from a fraction of a nanometer to about 100 nm [57]; with a minimum gap of approximately 20 nm, the fracture surfaces can get considerably closer than that.

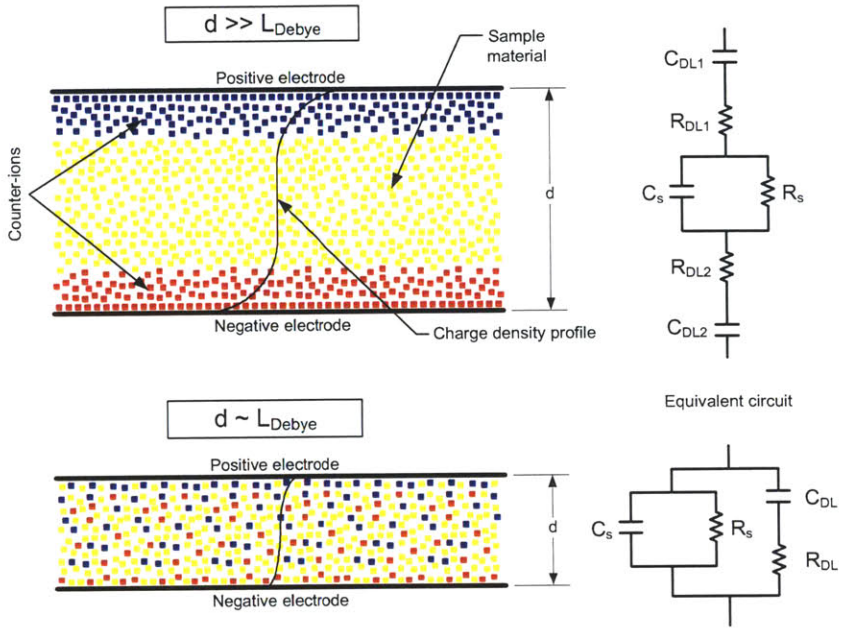


Figure 1-13: When the surface separation is large compared to the Debye length of the solution, the impedance of the sample is masked. Illustration courtesy of H. Ma, [87].

1.2.4 Molecular Filter

Figure 1-15 depicts the two different types of fracture surfaces employed as a molecular filter. The small gap precludes entry by the larger species in the mixture. This use of the fracture surfaces is reminiscent of the first Nanogate patent [130].

Because the size of the gap is controlled, different species are sorted by the same device, and if the gap does become clogged, the surfaces can be pulled all the way open for flushing. Potential applications for a molecular filter include the filtration of nitrogen and hydrogen. The purity of nitrogen gas is "the fundamental limiting factor for nearly every major new semiconductor material used today" [21, p. 12]. Likewise, hydrogen purity, where the principal contaminants are carbon monoxide, carbon dioxide, assorted hydrocarbons, and sulfur compounds, is very important for fuel cell performance [142]. "Fuel cells require hydrogen that is 99.999% pure, which today costs about $15 to $22 per kilogram" [40], with one kilogram of hydrogen delivering roughly as much energy as a gallon of gasoline. Unfortunately, these contaminants have characteristic dimensions in the single- to sub-nanometer range; too

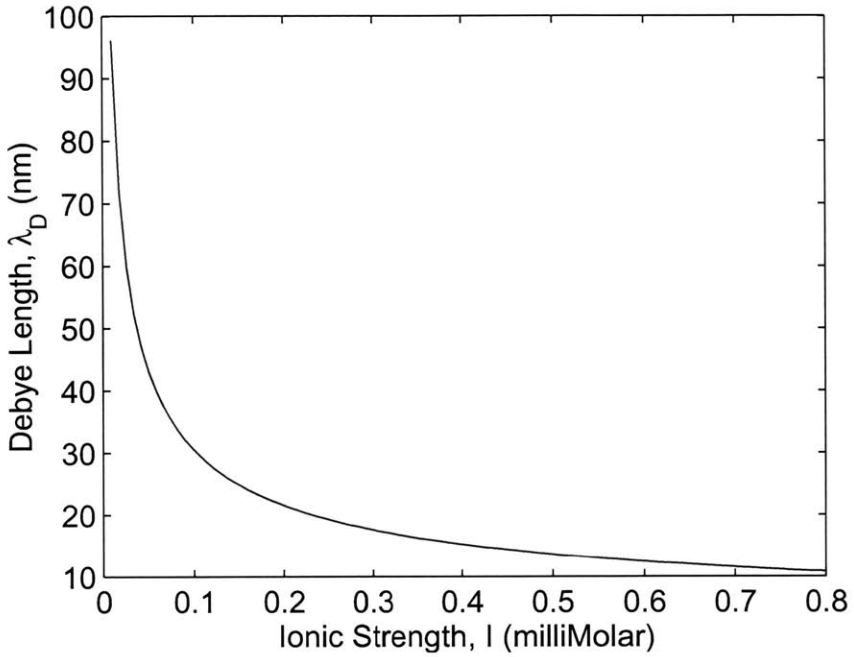


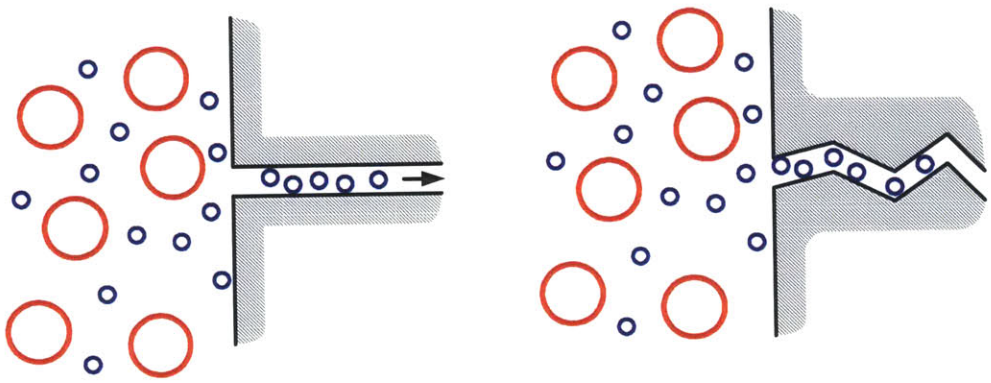
Figure 1-14: A plot of Debye length, λ_D, as a function of ionic strength, I (Equation 1.3)

small for a device with a minimum gap of 20 nm.

Large macromolecules are a better candidate. The Stokes' radii, a measure of a molecule's size based on its friction coefficient [36], of a number of common proteins are in Table 1.2. These proteins are likely to be too small for filtration by a device with a 20 nm gap (although given the labyrinthine nature of the fracture surface interface, surprising results are conceivable), but their larger cousins (some proteins are up to 100 nm in size) might be filterable.

1.3 Outline

The aim of this thesis is to develop a method and process for the fabrication of pairs of precision silicon surfaces embedded within a supporting compliant mechanism and a Micro Electro-Mechanical System (MEMS) that employs such surfaces as the separable plates of a variable capacitor. Once the design and process are perfected others could use it to explore the applications described.



(a) Nano-smooth planar surfaces

(b) Complementary surfaces

Figure 1-15: A molecular filter concept. Regardless of the gap geometry, its small size should facilitate sorting.

Protein	**Source**	**Molecular Weight (kDa)**	**Stokes' Radius (nm)**
ribonuclease A	bovine pancreas	13.7	1.64
chymotrypsinogen A	bovine pancreas	25.0	2.09
ovalbumin	hen egg	43.0	3.05
albumin (BSA)	bovine serum	67.0	3.55
aldolase	rabbit muscle	158.0	4.81
catalase	bovine liver	232.0	5.22
ferritin	horse spleen	440.0	6.10
thyroglobulin	bovine thyroid	85.0	8.50

Table 1.2: Proteins and their sizes, from [37].

Chapter 2 describes the development of the fracture process. After some early missteps, the single stage device in Figure 1-2(a) is developed. The (110) orientation is confirmed to produce fracture surfaces superior to the (100) orientation. Lithographically defined notches are found to be insufficiently sharp to prevent material ejection, and are replaced by Focused Ion Beam (FIB) notches, which are in turn replaced by anisotropically etched notches. The single stage device is reworked into a two-stage device with superior moment rejection properties in order to produce planar fracture surfaces. Complementary fracture surfaces are produced from a wide variety of specimen and notch geometries. The smoothest planar fracture surfaces are produced by 10 μm square specimens that have been anisotropically notched across their full width.

In Chapter 3, alternatives to fast fracture for the fabrication of surfaces are discussed. Stress corrosion cracking is a stress activated corrosion process that has been demonstrated to result in remarkably low surface roughnesses in silicon. The principal difficulty is preventing the onset of fast fracture as the crack propagates further and further througth the specimen, increasing its stress intensity factor. Anisotropic etching is used in Chapter 2 to make notches, but with properly oriented wafers, it can also create surfaces. Several test etches are done to produce etched surfaces equivalent to the fracture surfaces demonstrated in the previous chapter. The challenge of implementing a nano-gap with such surfaces is that because the device is normally open, the bearing that brings the surfaces into close proximity must be even more precise than the equivalent bearing for a normally closed fracture based device.

Chapter 4 covers the design of a variable capacitor device with fracture surfaces as the separable plates. As mentioned earlier, maximizing the capacitance by minimizing the stable displacement is a major challenge. A succession of more elaborate models is developed to describe the three-way force balance between the compliant structure's spring force, the actuator, and the capacitive force of the fracture surfaces. That the system is stable when the actuator is working against the structure's spring force, but not when working against the capacitive force is the principal physical insight.

Chapter 5 describes the fabrication and testing of the variable capacitor. In the

first prototype, a problem with blunting of the anisotropically etched stress concentrating notches is traced to an oxidation step necessary for the actuator. The fix developed for the second prototype, covering the notch with a nitride diffusion barrier to prevent oxidation, does not work. Dies extracted from the process before oxidation fracture well, and those fractured after oxidation do not, despite the confirmed absence of oxide in the notch. For the third prototype, the order is reversed, and the notch is etched after thermal oxidation. This switch produces somewhat sub-optimal notches, but adequate fracture surfaces.

Conclusions and some suggested avenues for future work are in Chapter 6.

Chapter 2

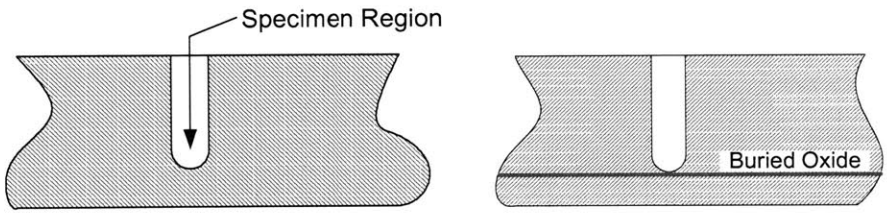
Fracture Process Development

To develop the precision surface fracture process, a series of devices were fabricated in the device layers of Silicon On Insulator (SOI) wafers. Though structurally elaborate, these devices were simple to fabricate (no more than two masking steps were necessary and no actuator was included), thus facilitating rapid experimentation.

A previous series of devices with an integrated zipper actuator [81] had proved to be un-manufacturable. In that concept, the specimen region, where the fracture was to occur, was fabricated by etching almost all the way through the wafer and then doing a second etch to define the actuator (Figure 2-1(a)). A few test etches made it clear that creating a specimen in this manner was unworkable. Without an etch stop, the etch depth could not be controlled, so the specimen geometry could not be controlled.

An alternative process with the specimen defined in the device layer of an SOI wafer and the zipper in the handle layer was developed (Figure 2-1(b)). This version was also un-manufacturable. The buried oxide layer of the SOI was not sufficient to protect the underside of the specimen during the long etch necessary to create the zipper in the handle layer.

The concept behind both the blind etch device (Figure 2-1(a)) and the etch-stop device (Figure 2-1(b)) was to fracture the specimen by amplifying the force from a thick zipper actuator with a lever (Figure 2-2(a)). Sadly, even if it had been fabricated, the device suffers from a serious flaw. As will be discussed in Section 2.1.2,



(a) Blind etch (b) Etch stop

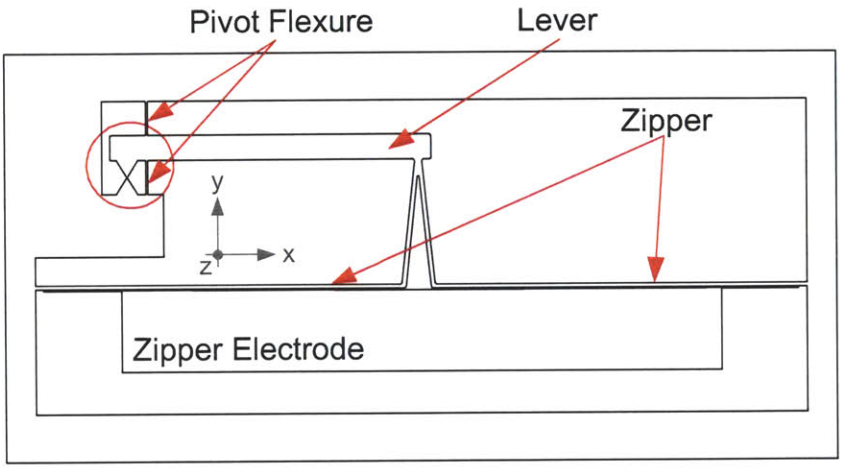
Figure 2-1: Blind etching was unsuitable for fabricating the specimen region because the trenches could not be inspected, especially at the high aspect ratio necessary for integration with the actuator. The buried oxide layer was not a strong enough etch stop to prevent damage to the specimen during etching.

moment loading of the specimen must be strictly limited to produce planar fracture surfaces. In this device, the lever mechanism produces substantial moment loading along the z-axis, and the off-center placement of the specimen produces moment in the x-direction. Other lessons learned from subsequent devices could be applied to the concept, the moment loading is an inherent problem.

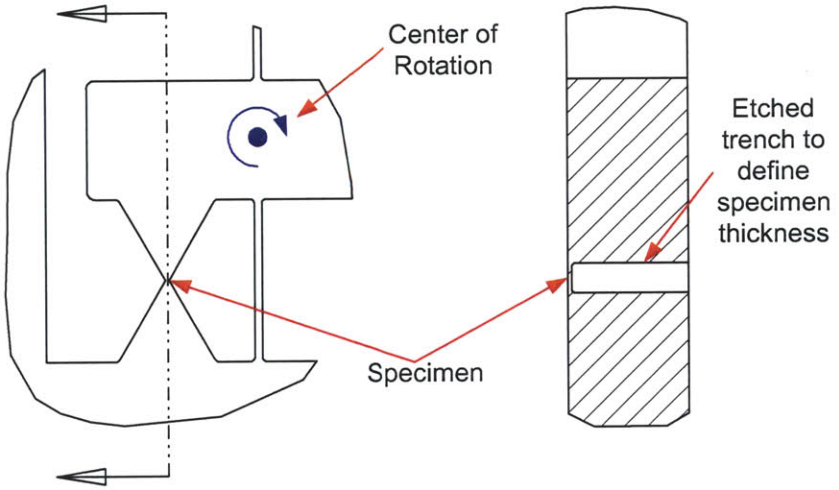
2.1 Single Stage Device

Fabricated in the device layer of an SOI wafer with a Deep Reactive Ion Etch (DRIE), the single stage device consists of a folded leg flexure [135, 134], a specimen, a set of stops, and a pair of probe holes (Figures 2-3 and 2-4). See Appendix A.1 for a complete description of the fabrication process. Pre-fracture, the flexure focuses the force applied by the probe at the specimen and functions as a linear bearing post-fracture. Finite Element Analysis (FEA) was employed to set the flexure and release-hole parameters so the stress at the specimen would be at least ten times the stress elsewhere.

The oxide beneath areas without holes is etched more slowly than the oxide beneath holed areas, leaving the solid areas anchored to the substrate. In this manner, the fixed portions of the flexure structure, the stops, and one end of the specimen remain fixed to the substrate. The stops prevent post-fracture flexure overtravel. The forces required to rupture the specimen are quite large (relatively speaking), and the



(a) View of the entire device



(b) Detailed view of the specimen region with cross section

Figure 2-2: Views of the unmanufacturable device concept. Note the moment loading of the specimen about the x and z-axes.

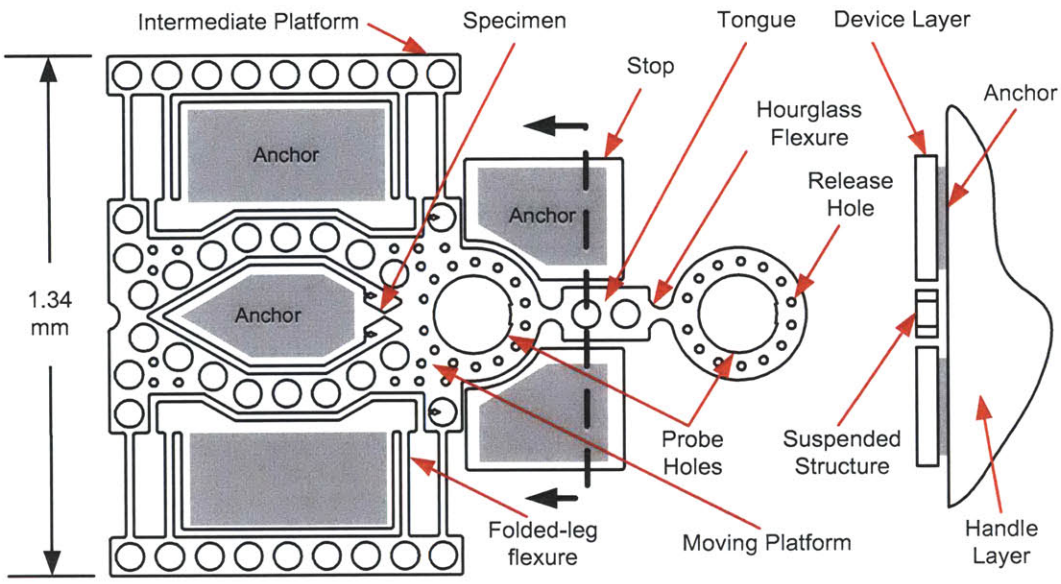


Figure 2-3: The single stage device. Holes through portions of the structure to be released speed the penetration of hydrofluoric acid (HF). The oxide beneath areas without holes is etched more slowly, leaving those area anchored to the substrate.

flexure would break if its post-fracture travel were not limited.

The specimen region is 10 μm across and its thickness is determined by the depth of the device layer; between 10 and 20 μm in this case. Each die contains devices with specimens at two different crystal orientations, (110) and (100). Silicon has three primary crystal planes, (100), (110), and (111). The favorable cleavage planes are the (110) and (111) [3], but given the negligible cost, it was thought worthwhile to experiment with the (100), especially since the (111) planes are inaccessible in the wafers used for this experiment.

The force to fracture the specimens is applied with an external probe. The tip of the probe is placed in one of the probe holes and moved to the right (Figure 2-4), fracturing the specimen in tension. The hourglass flexures on the tongue allow the rightmost probe hole to move normal to the direction of travel, preventing unnecessary strain.

Releasing the devices is somewhat problematic. The devices' characteristic dimension in-plane is much larger than its characteristic dimension normal to the plane of the wafer (1:100) or the thickness of the sacrificial oxide layer (1:2000), making

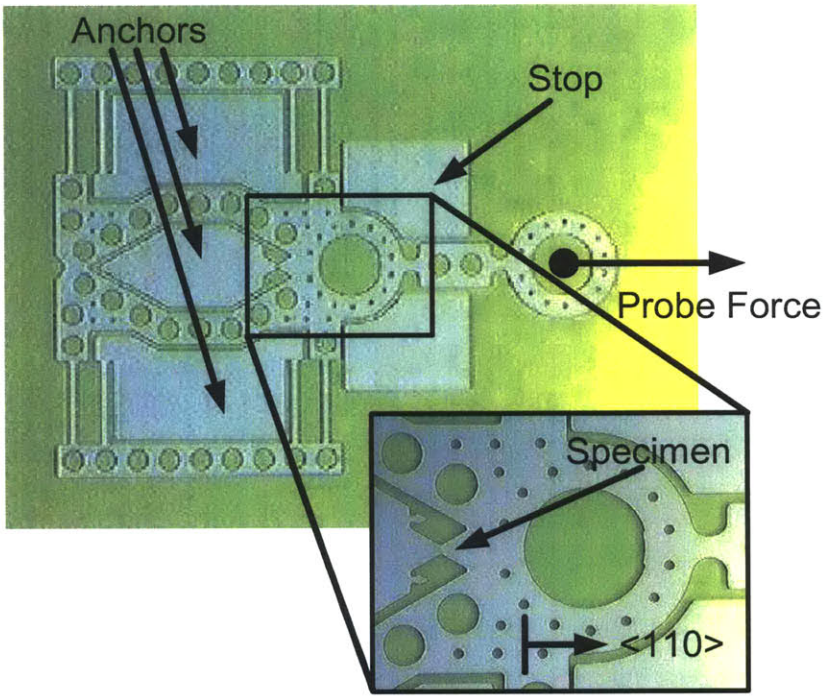
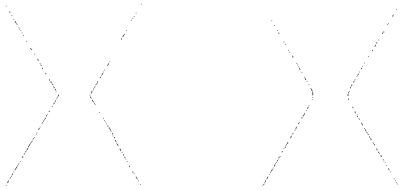


Figure 2-4: A picture of the fabricated single stage device. The oxide layer has not yet been etched to release the device. The small arrowheads to either side of the specimen region indicate the ¡110¿ direction.

it extremely vulnerable to stiction [92, 93] between the device layer and the handle layer. To overcome this difficulty, the release etch is arrested by diluting the acid with water and leaving the devices submerged post-release. The specimens are fractured underwater and then dried for analysis. There has been some success with methanol drying, but it could not be repeated. A vapor hydrofluoric acid release [54] was also attempted, but without a specialized setup, this too proved unworkable.

2.1.1 Lithographically Notched Specimens

The specimens are shaped like squared-off hourglasses. The hope was to concentrate the stress and approximate the sharpness of natural cracks. As drawn, the neck of the hourglass was not rounded (Figure 2-5(a)), but in the course of being made into a mask, transferred lithographically to the wafer, and then etched, the neck acquired a micron scale curvature (Figure 2-5(b)).



(a) Sharp ideal corners

(b) Round as fabricated corners

Figure 2-5: The specimen region, as drawn (a), and as fabricated (b).

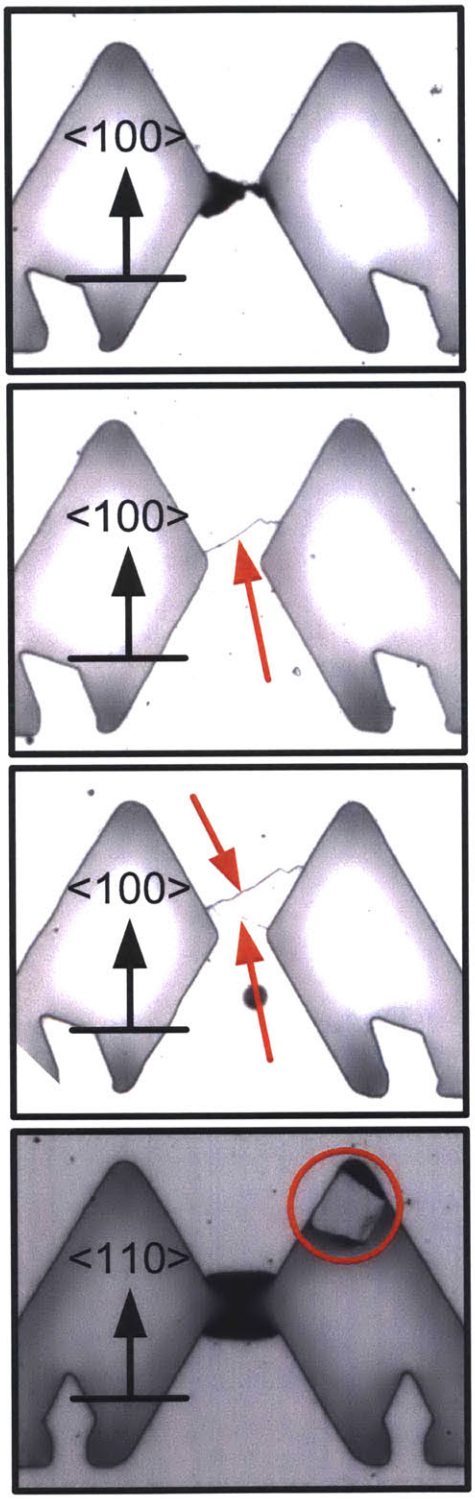
The hoped for fracture outcome was a mating pair of perfectly planar surfaces perpendicular to the wafer surface. Complementary surfaces would also be useful, and due to the absence of plasticity in silicon at room temperature [79, 113, 2, 17], they were expected to be relatively easy to produce.

Micrographs of some typical fractured specimens are in Figure 2-6. Specimens oriented with the (100) plane tended to produce rough surfaces and not fracture at the intended location. The (110) specimens did better, fracturing in the proper location and producing well ordered surfaces, but material was ejected.

Examining the (110) specimen from the lowermost panel with a Scanning Electron Microscope (SEM) (Figure 2-7) revealed generally planar surfaces with hackle marks radiating from the upper left corner of the lower fracture face. These marks are characteristic of a fracture initiation point [95, p. 502]. DRIE scallops are clearly visible on the side of the specimen (and elsewhere) in Figure 2-8, and may have provided the initiating stress concentration. The wedge of material ejected from the specimen is visible in the upper right, and a small complementary zone can be seen below the wedge ejection site.

It was not possible to determine whether the fracture surfaces are (111) planes. Measurement of the planes' angles made using SEM images was inconclusive. An angle of 66° was measured, not the 54.7° typical of (111) planes, but considering the method, errors of 10° are possible. The small size of the sample precludes the use of more standard methods for determining the crystal plane.

The troublesome ejection of material that prevents these otherwise good quality surfaces from mating is characteristic of a very high-stress fracture [55, p. 124]. This



Very uneven fracture surfaces with ejection

Uneven fracture surface not at desired location

Multiple uneven fracture surfaces not at desired location

Best of the lot, despite ejected material. Examined with SEM

Figure 2-6: Micrographs of typical lithographically notched fracture specimens captured with an optical microscope at 500X magnification.

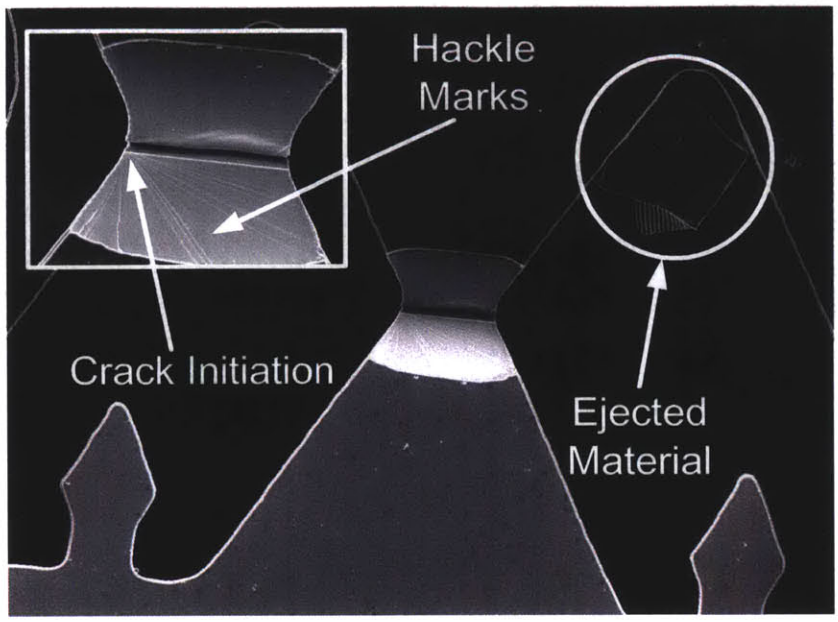


Figure 2-7: SEM micrographs of the lithographically notched specimen in the bottom panel of Figure 2-6. Note the hackle marks indicating the fracture initiated at the side of the specimen.

is commensurate with the relatively low stress concentrating power of the lithographic notch and the DRIE scallops. Thus, a better stress concentrator is needed to prevent material ejection.

2.1.2 FIB Notched Specimen Results

To prevent material ejection by more intensely concentrating the stress, several specimens were notched with a Focused Ion Beam (FIB) (Figure 2-9). The ion current was set to 100, 30, and 10 pA. The 30 and 10 pA settings resulted in equally sharp notches with radii of approximately 5 nm, which compares favorably with silicon's atomic radius of 0.1176 nm. The 10pA notch was somewhat asymmetric. All cuts were made to a set depth of 1 μm. The depth of the notch increases near the edges of the specimen (Figure 2-10), but the black streak extending down most of the side of the specimen is not the cut itself, but an artifact.

As had been hoped, the specimens notched with the FIB fractured without ejecting any material (Figure 2-10). Unfortunately, the fracture was not planar, merely

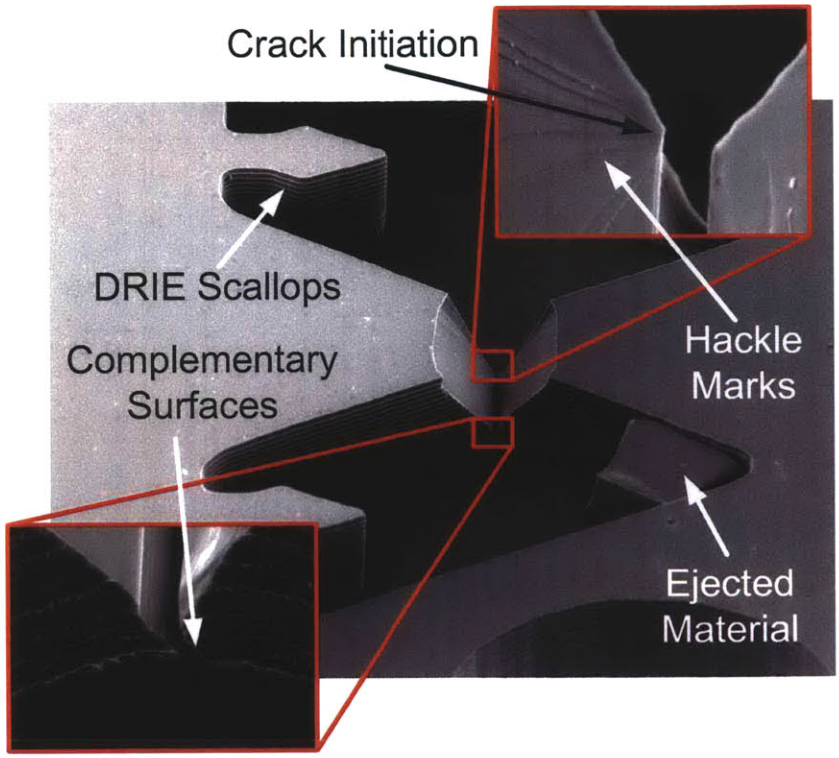


Figure 2-8: Oblique SEM micrographs of the specimen in Figure 2-7. Fracture most likely initiated at a DRIE scallop.

complementary.

The fracture came down the FIB notch for about 2 μm below the tip of the notch and then started to move along a different, slightly curving, line. A curved fracture surface is indicative of a specimen broken under the influence of both tension and moment rather than pure tension [4].

Specimen Loading Analysis

FEA confirmed the specimen was subject to substantial moment loading (Figure 2-11, Figure 2-12) due to imprecise probe placement (Figure 2-13). The abscissa of the plots is probe position, measured normal to the wafer plane from the middle of the device layer. Because the experimental setup did not allow for precise positioning of the probe normal to the wafer plane, positions ranging from the top to the bottom of the device layer were simulated. The symmetry of the results about the mid-plane

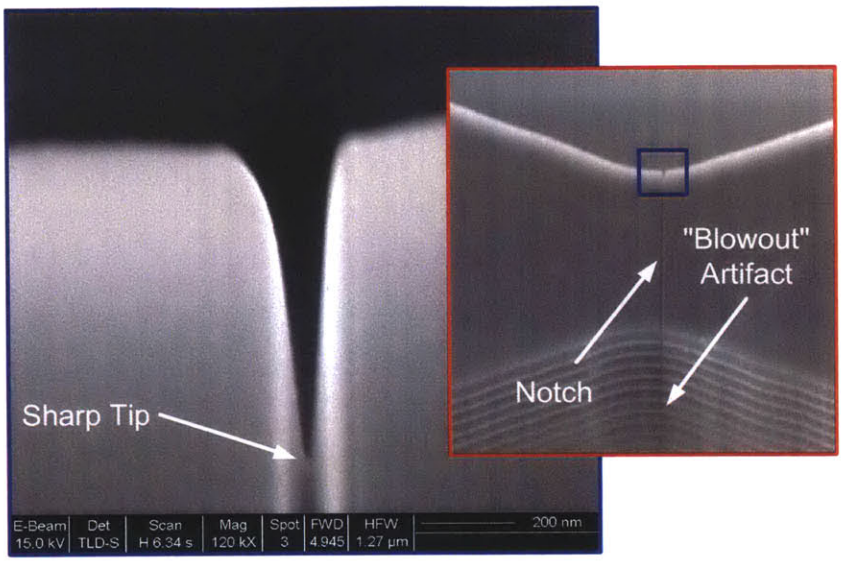


Figure 2-9: A specimen with a FIB (30 picoamp) notch. Note the approximately 5 nm tip radius of the notch. The atomic radius of silicon is 0.1176 nm.

of the device layer parallel to the wafer plane indicates the structure is insensitive to being anchored only on the bottom side of the device layer.

The stresses were calculated by constraining the specimen and solving for the reaction moments and forces. The reaction force, F_r, was divided by the specimen area, A_s, as an estimate of the tensile stress, σ_t given by

$$\sigma_t = \frac{F_r}{A_s}. \tag{2.1}$$

The reaction moment was converted to a bending stress using the standard beam relation (distance from the neutral axis, c, was set to the maximum, half the device layer thickness) resulting in

$$\sigma_m = \frac{M_r c}{I_{xx}} \tag{2.2}$$

The results for the single stage device (the reference design, "Ref") are marked with circles. The stress is purely tensile if the probe pushes at the center of device

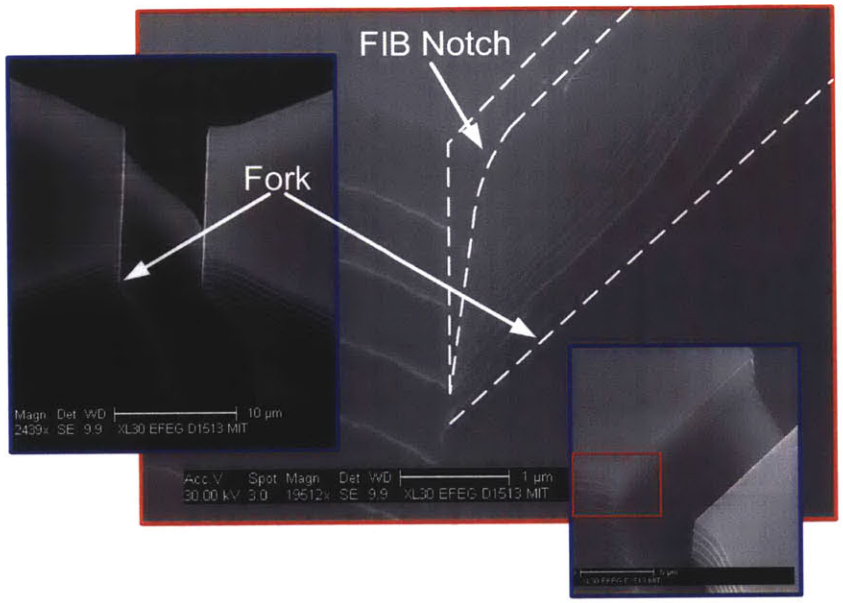


Figure 2-10: SEM micrographs of a FIB (30 picoamp) notched specimen. The fracture moved along the FIB notch for a few microns and then shifted.

layer. As the probe is moved away from the center of the device layer, however, the stress due to bending increases and the tensile stress decreases until the stress due to bending is greater than that due to tension.

The principal component of the reaction moment, M_r, is M_x, while the principal component of the reaction force, F_r, is F_z. The normalized residual force and moment plots are created by dividing the difference between principal reaction component and the reaction magnitude by the reaction magnitude:

$$|M_{residual}| = \frac{M_r - M_x}{M_r} \tag{2.3}$$

$$|F_{residual}| = \frac{F_r - F_z}{F_r} \tag{2.4}$$

$|F_{residual}|$ and $|M_{residual}|$ are a measure of the significance of the secondary force and moment components. The relative importance of the secondary force components, F_x

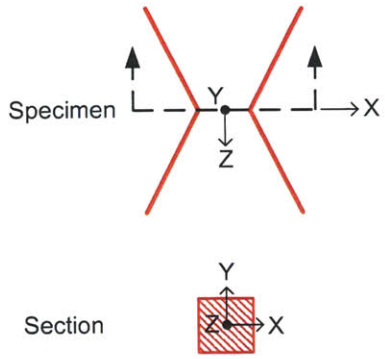


Figure 2-11: Specimen coordinate system for use with the FEA results in Figure 2-12. Y is the direction perpendicular to the wafer surface. Z is the direction in which tension is applied.

and F_y, is always small, but grows when the probe is pushing far from the centerline. The relative magnitude of the secondary moment components, M_y and M_z grows as the probe moves closer to the centerline because the primary moment, M_x, is going to zero.

These results motivated the development of the two stage device, discussed in the next section, which was designed to attenuate moments and load the specimen more purely in tension.

2.2 Two-Stage Device

The single stage device was redesigned to reduce the moment induced stress. The new design is shown without release features in Figure 2-14. As in the previous design, the probe is coupled to the device with a pull ring. From there, the input flexure absorbs some of the moment inadvertently generated by the probe position. A long slender member intended to serve as a string capable of transmitting only tension connects the input flexure to the specimen flexure, which further attenuates moment and guides the specimen post-fracture. More beams have been added to both the input and the specimen flexures to increase their moment stiffness. Where there was one beam before, there is now a cell of three in parallel. The FEA results for the new design are in Figure 2-12, marked with squares. The stress from moment loading has

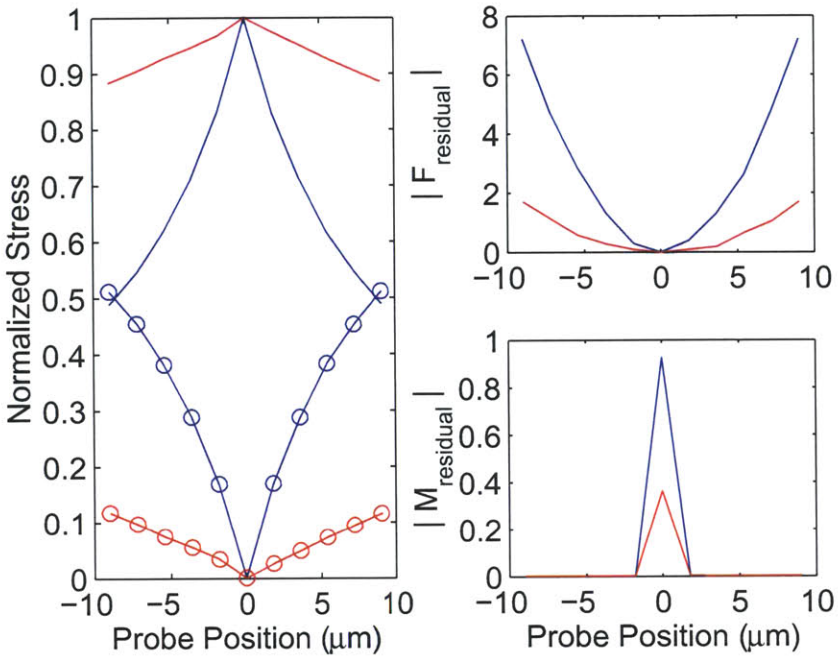


Figure 2-12: FEA results indicating the relative magnitude of moment stress vs. tensile stress.

been significantly reduced.

To facilitate post-fracture examination of the specimens, a latch was added to the device (Figure 2-15). After the specimen is fractured, the flexure travels all the way to its stops and engages the latch, locking the device in an "open" position more amenable to SEM study.

2.2.1 Lithographically Notched Specimen Results

The results from fracturing lithographically notched two-stage devices were unremarkable. Most lithographically notched devices fractured at places other than the specimen zone, e.g. the pull ring, the pull ring tongue, or the tether. Devices that fractured in the specimen region did so in the same fashion as the lithographically notched single stage devices: by ejecting material (Figure 2-16). Both results testify to the poor stress amplifying power of the lithographic stress concentration and confirm the necessity of sharply notching the specimen.

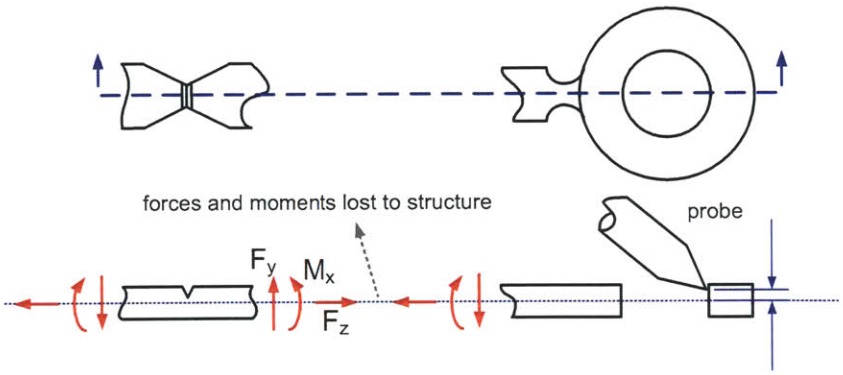


Figure 2-13: If the probe is not aligned with the mid-plane of the device layer, a moment is created and transmitted through the structure to the specimen.

2.2.2 FIB Notched Specimen Results

The results from fracturing FIB notched specimens were considerably more interesting. A chevron shaped (Figure 2-17), rather than straight, FIB notch was used [4]. The chevron notch is made by varying the dwell time of the beam on different parts of the line it is following across the specimen. A longer dwell time produces a deeper cut. A good chevron notch has the advantage of concentrating the stress at a particular point at the center of the specimen rather than along the whole line. This increases the likelihood the fracture will initiate at the center, enlarging the area over which the fracture is moving relatively slowly. Cracks accelerate as they move away from their point of initiation and a faster crack makes a rougher surface [95, p. 502], so the area near where the crack started often has the best surface finish.

Two of the four specimens fractured cleanly; the other two split, ejecting material. The origin of this difference is unknown. One would expect FIB notches made under the same conditions to be equally good at concentrating the stress. Regardless, both morphologies yielded useful results.

Several views of a cleanly fractured specimens can be seen in Figure 2-18. Unlike the equivalent fracture surfaces of the single stage devices (Figure 2-10), these surfaces are planar, indicating the device has successfully isolated the specimen from stray moments. The small bumps on the surface are believed to be contaminants. The experimental setup necessitated that the specimens be exposed to numerous unclean

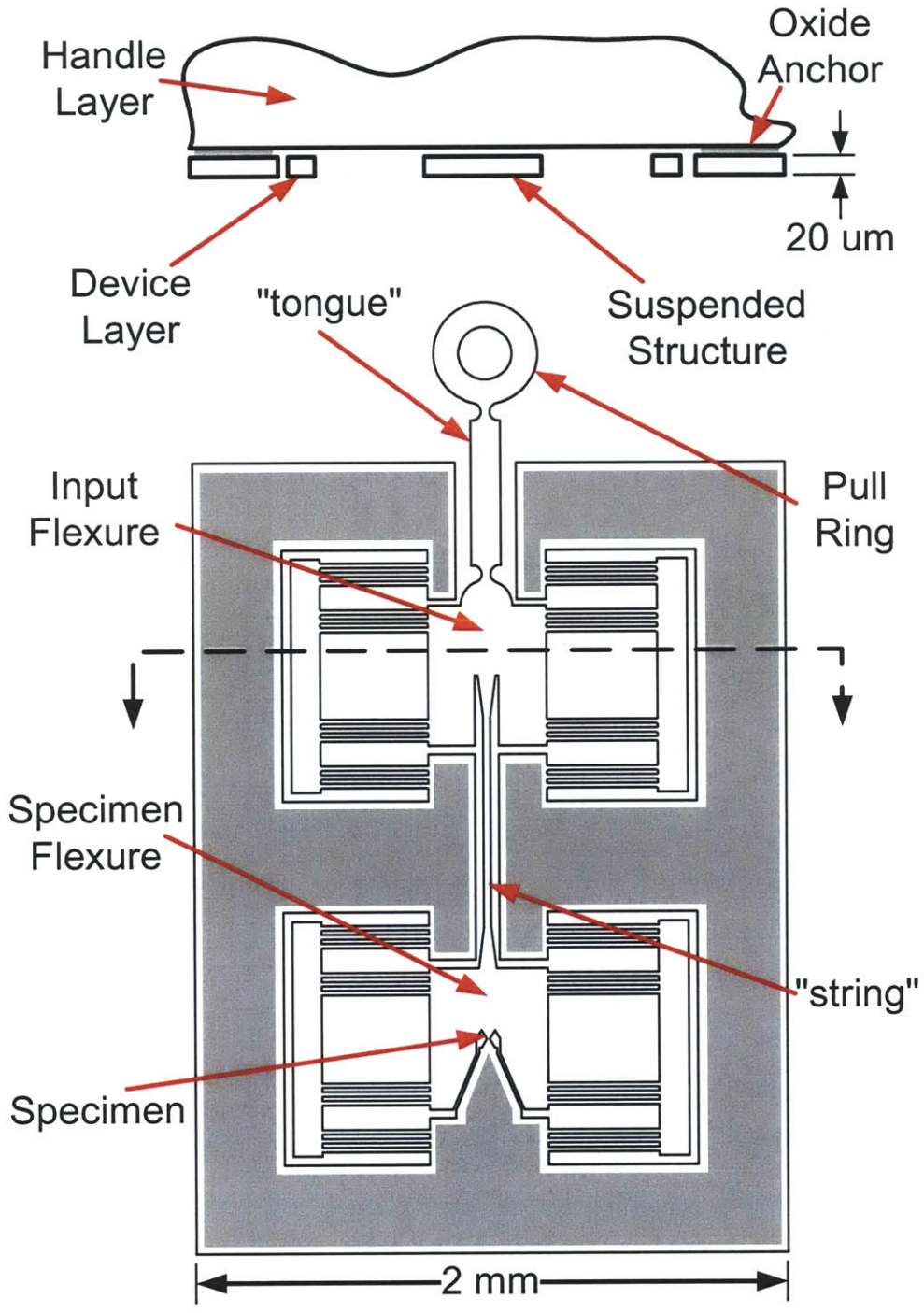


Figure 2-14: The two stage device. For clarity, the release-holes and the latch mechanism are not shown. The gray area is anchored to the substrate.

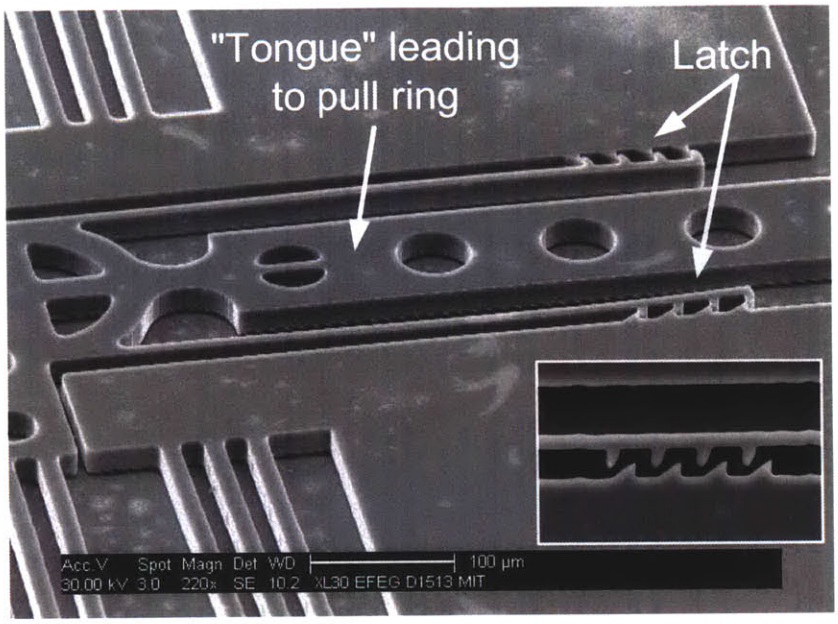


Figure 2-15: Latch mechanism to facilitate post-fracture examination of the surfaces. Inset is a top view of a slightly different version of the latch.

environments between fracture and SEM examination.

It is not known for certain what plane the fracture follows. It could be a (111) plane, but instruments for determining crystal orientation lack the spatial resolution necessary to confirm this [136]. Measurements from SEM images give an angle of 61°, close enough to the 54.7° of the (111) plane to be suggestive, but not definitive. Measurements with a Tunneling Electron Microscope (TEM) could perhaps resolve the issue, but the thickness of the sample precludes such a study.

The hackle lines radiating from one corner of the surface indicate the chevron notch has been ineffective at making the fracture initiate at the center of the specimen. It is unclear how important this is, as the whole surface is quite good. The fracture may have initiated at the side of the specimen because the chevron notches differed less from straight notches than desired (Figure 2-19).

The ratio of the depth at the center to the depth at the edge is only 1:2, instead of the 1:5 or 1:10 [22, p. 126] typically seen in meso-scale specimens. The low ratio could not be changed by using a more lopsided dwell profile or by increasing the number of passes, indicating the aspect ratio limit of the FIB has been reached. Additional

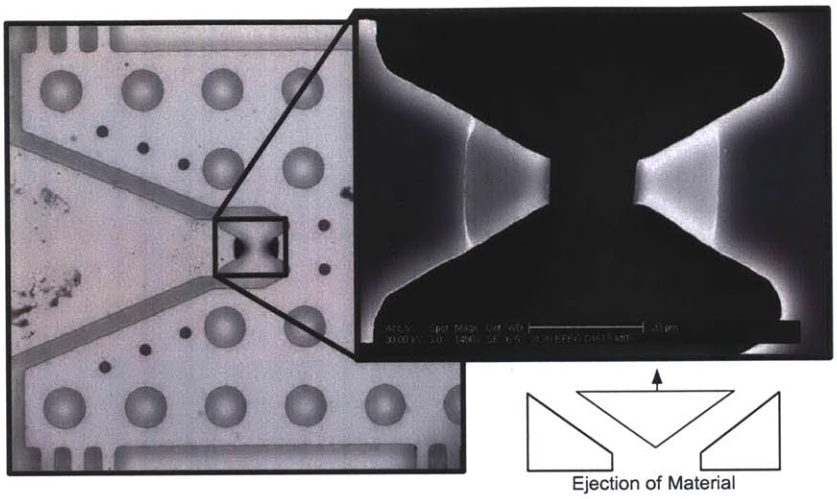


Figure 2-16: One of the rare lithographically notched two stage devices that fractured in the specimen zone. The ejected material is not visible.

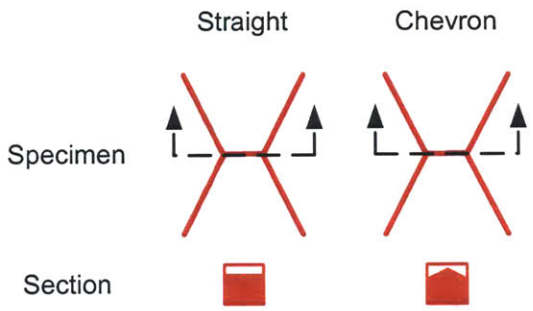


Figure 2-17: The two types of FIB notches employed.

material can be milled from the bottom, but because it cannot escape from the bottom of the trench, it is re-deposited. This sort of phenomenon is not unheard of; researchers attempting to fabricate nanopores have seen their pores close during what was intended to be milling operation [80, p. 166]. The fracture's tendency to run vertically and then fork (Figure 2-10) may be related to such a re-deposition or flow phenomenon or to ion damage of some other sort. It might have been possible to mill deeper by widening the cut, but rastering the beam to do so would have also blunted the notch.

The notch also has a few anomalous features: a semi-circular depression at its center and a dramatic increase in depth at the extreme edges. The origin of the

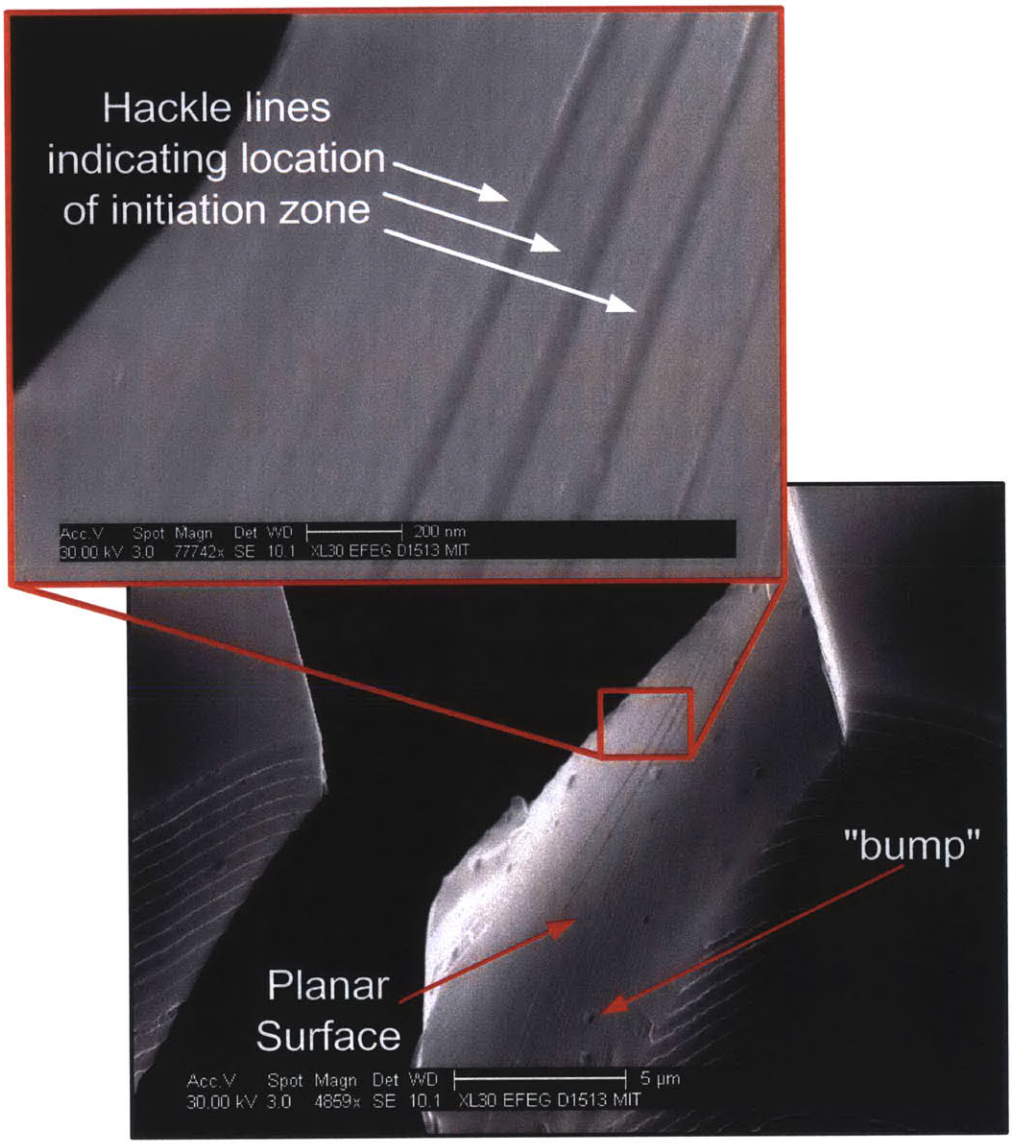
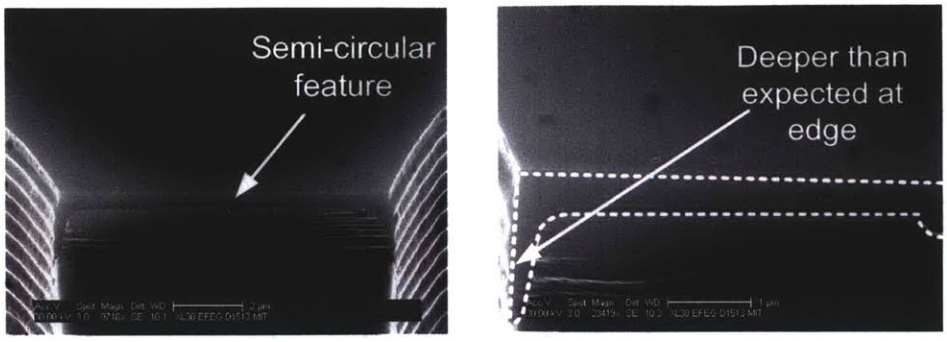


Figure 2-18: The cleanly broken notched specimens. The fracture persists in initiating at the DRIE scalloped side of the specimen, but the planar surface indicates that stray moments are being rejected by the structure.



(a) 300 Cycles (b) 1000 Cycles

Figure 2-19: Micrographs of the chevron FIB notch. The notch can only be investigated post-fracture.

semi-circular feature is unknown, but the dramatic increase in depth near the edge of the specimen is likely inherent to the FIB process. For the same reasons that edges appear unusually bright in SEM images, ion milling will tend to produce blowout features near edges; material that would normally be displaced is ejected when near the edge because there's nothing to stop it.

Micrographs of a specimen that fractured poorly are shown in Figure 2-20. Ejecting material is bad from a device perspective, but these images do support the contention that the fracture surfaces are complementary. With essentially no guidance – the wedge is fully separated from the flexure, the gap between the ejected wedge and the rest of the structure closes almost completely.

Two devices oriented to the (100) crystal plane were also fabricated, notched, released, and fractured. The micrographs in Figure 2-21 show the results for one specimen; the other, not pictured, ejected material. The fracture surfaces are not nearly as good as those produced by specimens oriented to the (110) plane. Both specimens were notched in the same manner as the (110) specimens, and like them, the fracture seems to have initiated at the side of the specimen. These results confirm that the (100) planes make poor cleavage planes.

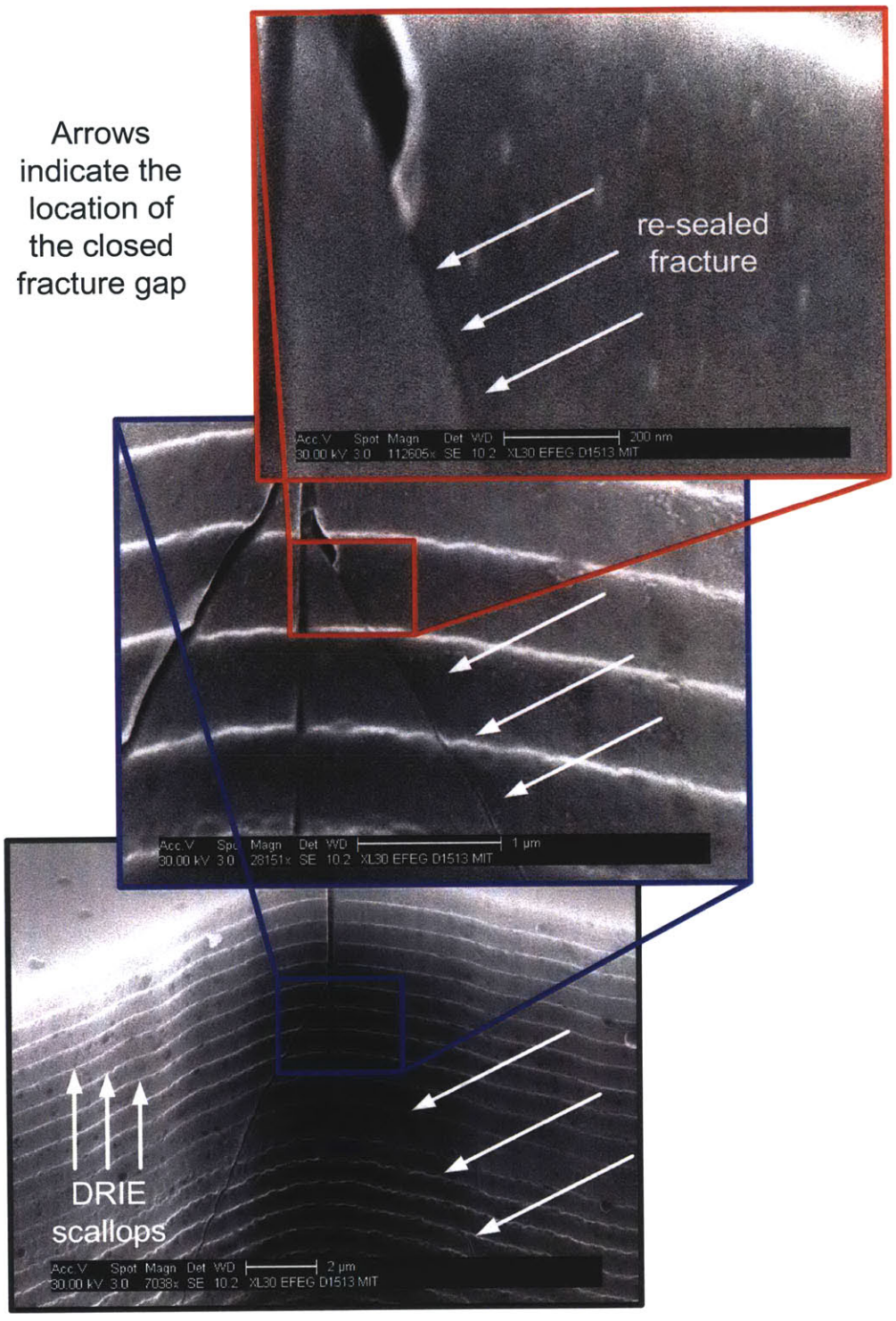


Figure 2-20: Micrographs of a specimen that fractured in multiple locations. Note how remarkably the surfaces re-seal, indicating their extreme complementarity and the success of the flexure bearing at guiding their approach.

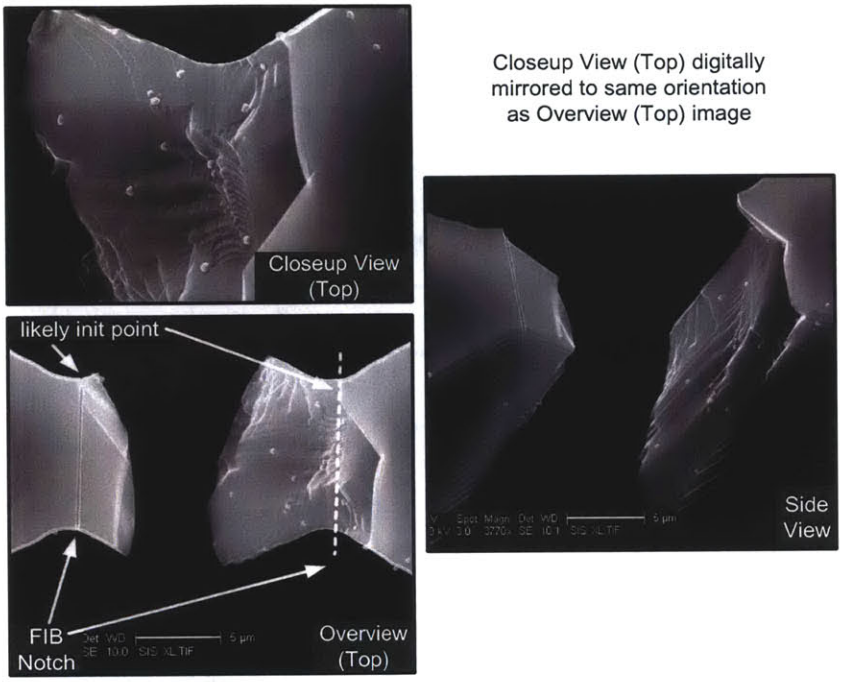


Figure 2-21: Micrographs of a specimen fabricated on the (100) plane and then FIB notched. The fracture surfaces are not nearly as good as those of specimens oriented to the (110) plane.

2.2.3 KOH Notched Specimen

Potassium Hydroxide (KOH) notching is an attractive alternative to FIB notching. Unlike notching with the FIB, it is a parallel operation – an entire wafer of devices can be notched at the same time. Also, alignment of the notch with the crystal structure of the specimen is guaranteed. Prior to this series of KOH notched devices, notches were aligned to the device, which had in turn been aligned to the wafer flat, which is only aligned to the wafer's crystal structure to within $\pm 1^{\circ}$ [34, 33].

KOH etches silicon's (111) planes hundreds [71] of times more slowly than the others. This anisotropy, produces self-terminating trenches with very sharp bottoms (Figure 2-22). It also undercuts features not perfectly aligned with the crystal structure of the wafer, leaving behind perfectly aligned trenches (Figure 2-23) [124, p. 64].

The strange artifact protruding from the side of the specimen (Figure 2-22) is a consequence of photolithography. A fluoroscopic examination of a second wafer

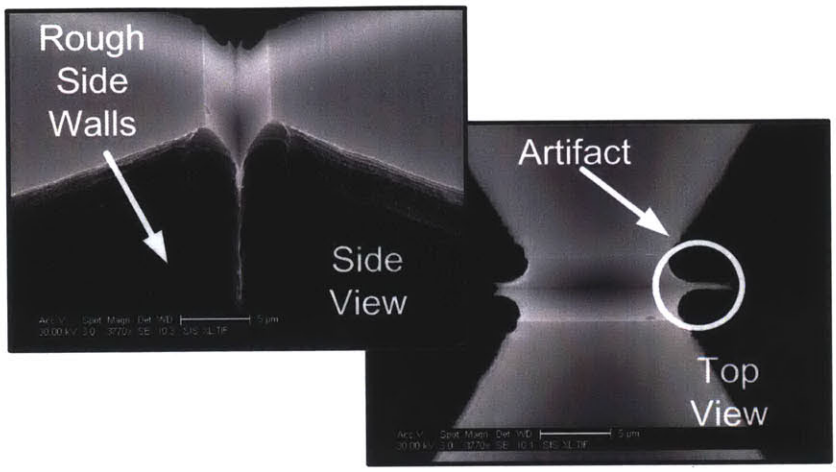


Figure 2-22: The KOH notch in an unbroken specimen. Note the sharp bottom for concentrating the stress.

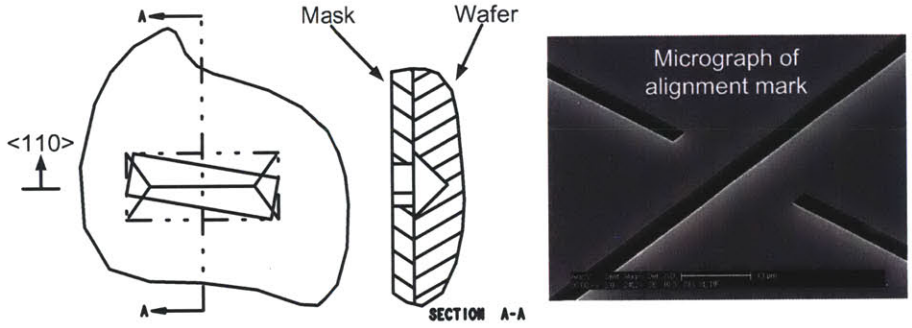


Figure 2-23: Anisotropic KOH etch undercuts mask features, creating alignment marks, or notches, perfectly aligned to the crystal structure of the wafer.

processed in parallel with the wafer from which these devices came but never DRIE'd revealed KOH trenches filled with resist. Unlike a standard microscope, a fluoroscope images only resist. Resist likely pooled in the trench during spin coating and was then not properly exposed due both to its greater than nominal thickness and being slightly out of focus because it is below the wafer plane. This poorly exposed resist did not dissolve as it should during development, leaving a thin layer that the etcher only partially etched through. The particular DRIE recipe used, MIT69A (Appendix A.2), does not typically produce such rough sidewalls (Figure 2-22); this photolithography error may explain the unusual results this time.

There is surprisingly little discussion in the literature of the sharpness of KOH

trenches. The only experimental result available is 5 nm [50], but as that measurement was made with an AFM, it is quite possible the authors were really measuring their AFM tip's radius of curvature.

Based on the amount of deflection in the probe at fracture, notching with KOH considerably reduces the force necessary to fracture the specimen. Limitations of the experimental setup prevent quantification of this effect, but it is there. The force is likely even less than that necessary to fracture FIB notched specimens; Reductions by a factor of four have been reported elsewhere [2].

Of the twelve devices fractured, eleven fractured at the specimen, and one broke at the pull-ring attached to the input stage, a failure that may have been due to experimenter error. None of the specimens ejected material, indicating a low stress fracture, which correlates well with the low fracture force observation.

As with previous devices, it was easy to open and close the specimens post-fracture (assuming the latch had failed or been deliberately degraded). No stiction or re-bonding was evident; immediate formation of a native oxide likely passivates the surfaces.

The fracture surfaces follow the (110) plane normal to the wafer surface. Unlike the FIB notched specimens, the fracture surfaces exhibit the classic mirror, mist, and hackle zones, progressing from one to the other as the crack accelerates away from where it was initiated (Figures 2-24 and 2-25) [95, p. 502].

Because the fracture is perpendicular to the surface, both faces can be examined, and they appear complementary (Figure 2-26). On devices where the latch failed, further evidence the surfaces are complementary can be seen, e.g. Figure 2-27 where the fracture faces have re-seated well enough that the gap between them cannot be seen. Unlike the FIB notched surfaces in Figure 2-20, both surfaces here are guided.

A second set of devices was designed to experiment with different KOH notch geometries (Figure 2-28). Specimens for both the (110) and (100) planes were fabricated. The (110) specimens were fully, partially, and pyramidally notched. The (100) specimens were only notched with pyramids, the nature of the KOH etch precluding the other types. Different DRIE recipes were used in an effort to make the sidewalls

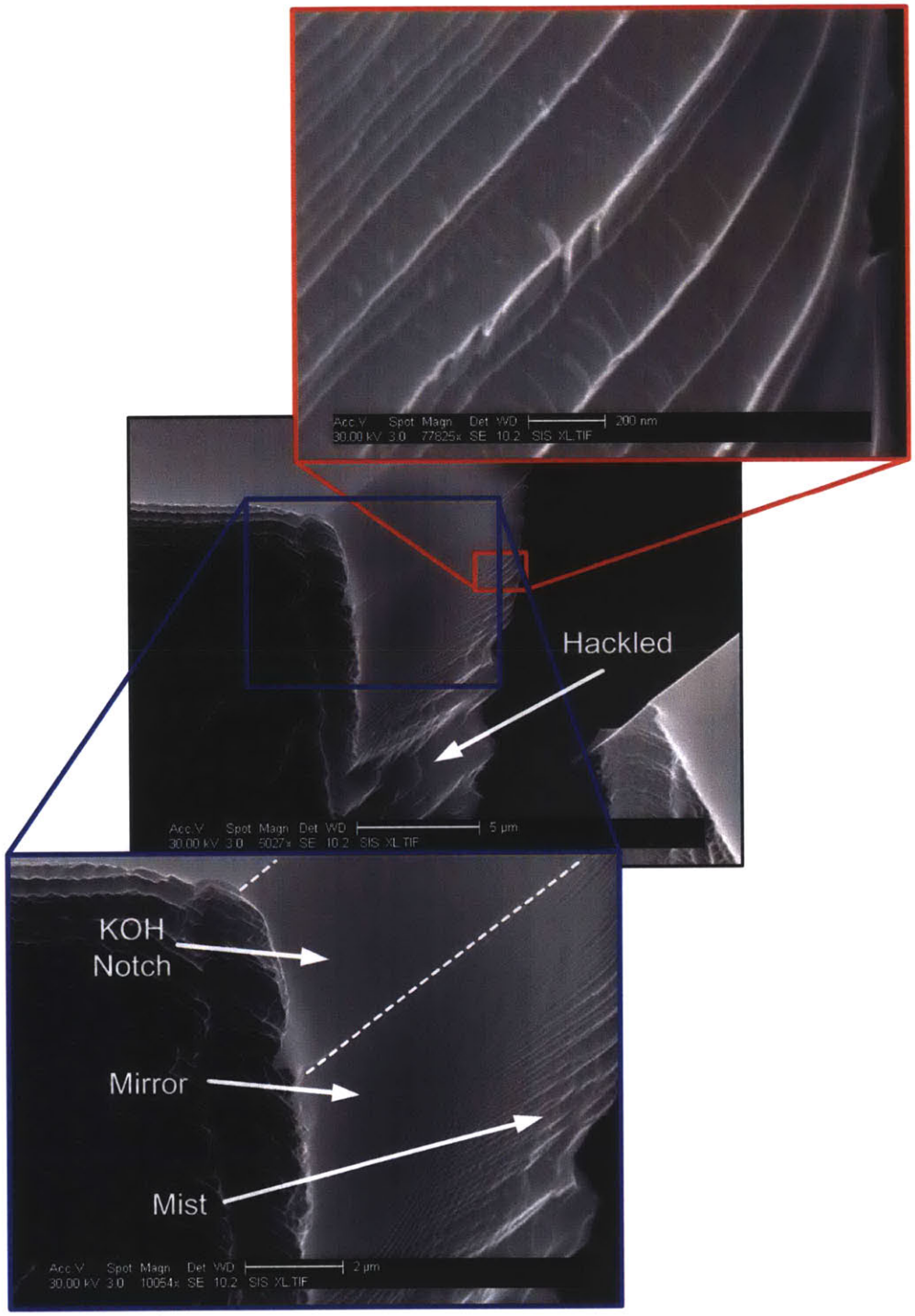
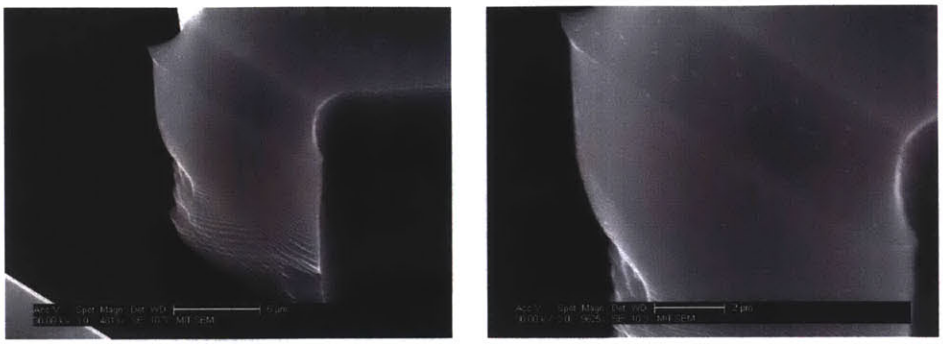


Figure 2-24: A series of micrographs examining one of the fracture surfaces from a KOH notched specimen. Note the classic mirror, mist, and hackled regions.



(a) (b)

Figure 2-25: An unusually good KOH notched fracture surface

smoother. Best results were seen from a recipe (STS-SHAL) that continuously etches and deposits passivating teflon without multiplexing (Figure 2-30).

Pyramid Notch (110) – Figure 2-28(c): The results from fracturing (110) type specimens with a pyramidal notch can be seen in Figure 2-29. They are not very good. The surfaces are not planar and material is ejected.

Partial Notch (110) – Figure 2-28(b): The results from fracturing a partially notched specimen can be seen in Figure 2-30. The extent of the notch is highlighted by the dashed lines. The faces are likely complementary but are not at all planar and are certainly not better than the results from fully notching the specimen. Note the smooth specimen sidewall surface of the DRIE etch, achieved by not multiplexing.

Full Notch (110) – Figure 2-28(a): The results of fracturing a 10 μm square specimen can be seen in Figure 2-31. Almost all of the surface is exceptionally smooth. The hackled region at the bottom of similar 20 μm specimens has been effectively removed. The crack passes all the way through the smaller specimen before accelerating to the speeds that roughen the surface. This configuration produces the best surfaces in terms of planarity and surface finish.

Pyramid Notch (100) – Figure 2-28(d): Figure 2-32 shows the results of fracturing a pyramid notched (100) specimen. One of the specimens turned out

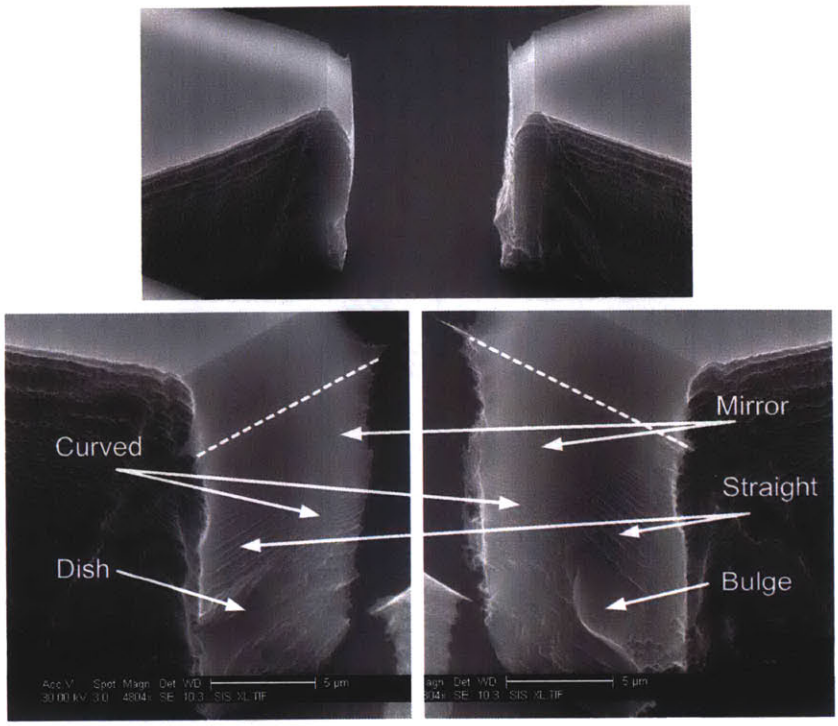


Figure 2-26: Micrographs of the same specimen from different angles. Note how the topographic features of the complementary surfaces correspond.

relatively well, reminiscent of the 20 μm specimens fractured with a full notch, but the other specimen shows a more typical result. It's also clear from the figure that the notches were not placed exactly in the middle of the specimen. The Electronic Visions EV620 mask aligner cannot do much better than $\pm 3\,\mu$m and putting a pyramid notch in the center of a specimen is a much less forgiving operation than making a full notch across a specimen.

2.3 Fracture Process Summary

Table 2.1 summarizes the results of experimenting with the different specimen configurations. The best results are from fracturing a 10 μm square (110) specimen with a full width KOH notch. The second best result is from fracturing (110) specimens with a FIB notch.

No results are available for (111) type specimens because special wafers would

Notch Type	Specimen Orientation (100)	(110)	(111)
No Notch	non-planar (Figure 2-6)	material ejection (Figure 2-8)	not performed
FIB Notch	non-planar (Figure 2-21)	planar and smooth (Figure 2-18)	not performed
Full KOH Notch	not performed	planar and smooth (Figure 2-31)	not performed
Partial KOH Notch	not performed	rough, non-planar (Figure 2-30)	not performed
Pyramid KOH Notch	non-planar, complementary (Figure 2-32)	rough, non-planar, material ejection (Figure 2-29)	not performed

Table 2.1: Summary of results. The best result is from 10 μm square specimens fully notched with KOH.

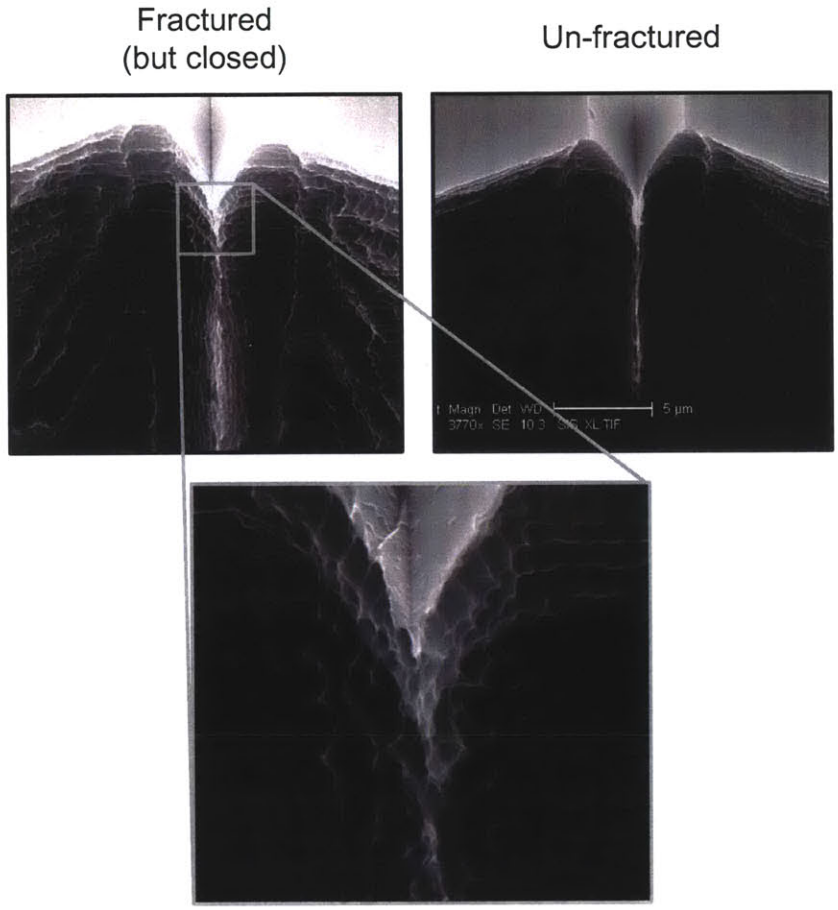
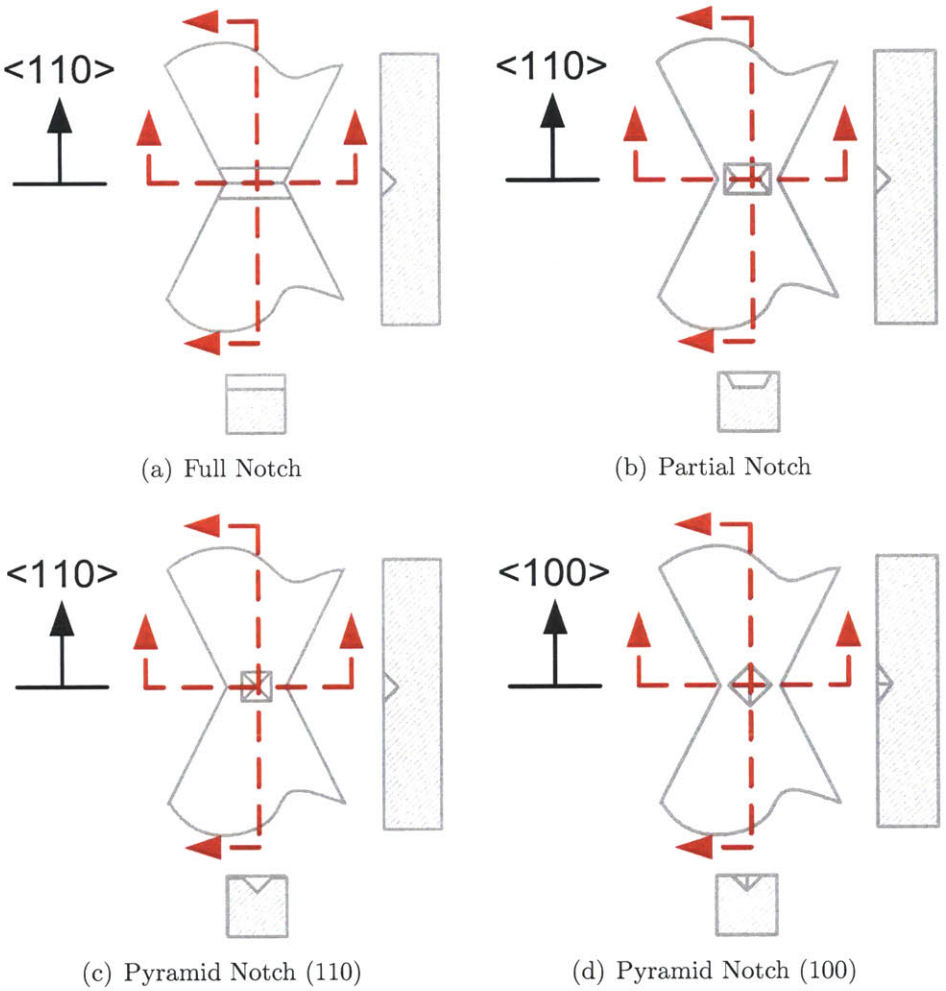


Figure 2-27: Fractured (but closed) and un-fractured specimens. The fracture interface cannot be seen, although that may be as much a consequence of high sidewall surface roughness as good sealing properties.

be required, and if they were obtained, it is unclear whether KOH notching would be effective. KOH etching the (110) wafers that would be used to produce (111) specimens produces channels with vertical rather than converging sidewalls. Without KOH, the only notch available would be FIB.

Full and partial KOH notching was not attempted for the (100) type specimens because the notches would be unstable during etching. Larger, undercut pyramid style notches that are aligned to the (110) plane would be produced. It is possible that some form of mask corner compensation [31, 38, 94, 122] could be used to produce approximately the correct shape, but the bottom of the trench would not be sharp.



(a) Full Notch

(b) Partial Notch

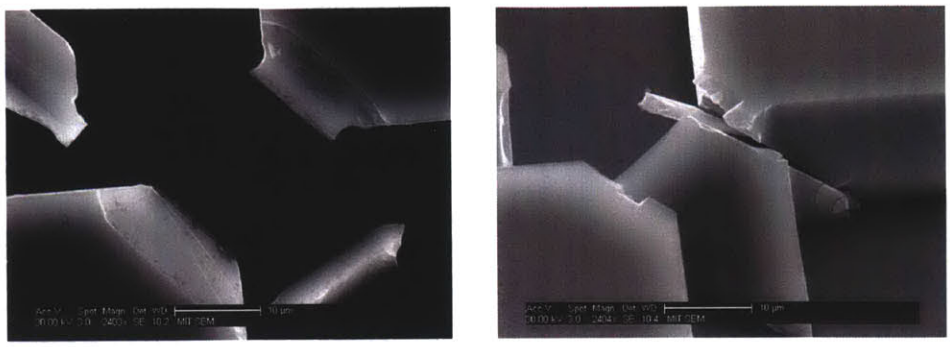
(c) Pyramid Notch (110)

(d) Pyramid Notch (100)

Figure 2-28: Types of KOH notches.

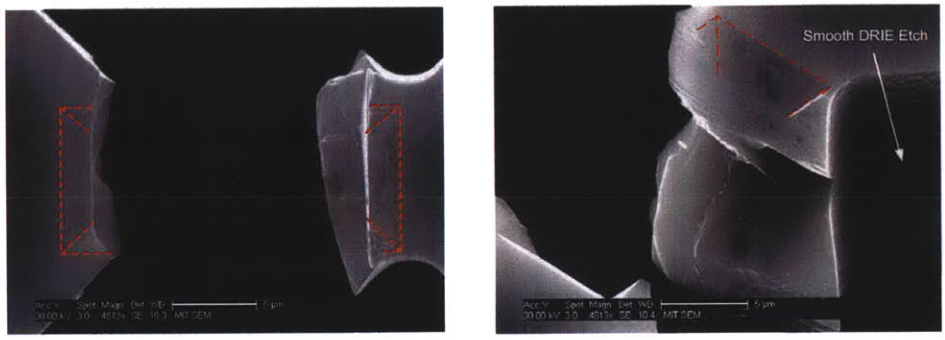
2.3.1 KOH Etched Sidewalls

A set of devices was designed that used KOH to etch the sides of the specimen as well as the notching trench (Figure 2-33). Unfortunately, the design was not fabricateable. Only a very thick photoresist (AZ4620) could be made to flow over the KOH etched specimens and the extreme length of the exposure required by the resist pooled around the specimen overexposed other portions of the pattern. Spray application of a thin resist (OCG825) also failed; during baking, the resist pulled away from the edges of the trench, leaving them exposed.



(a) (b)

Figure 2-29: Two examples of a pyramid notch fracture with a (110) specimen. Both ejected material, though especially in the righthand image, the surfaces are quite smooth and planar, reminiscent of FIB notched specimens.



(a) (b)

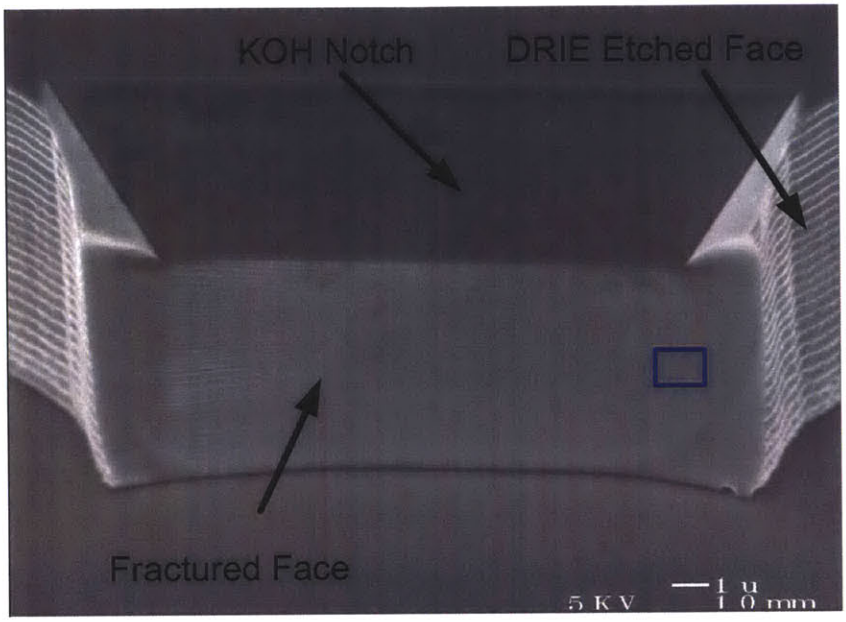
Figure 2-30: Partial KOH notch results. The notch is highlighted in red. Note the smooth specimen sidewall surface of the DRIE etch, achieved by not multiplexing.

2.4 Other Potential Notching Techniques

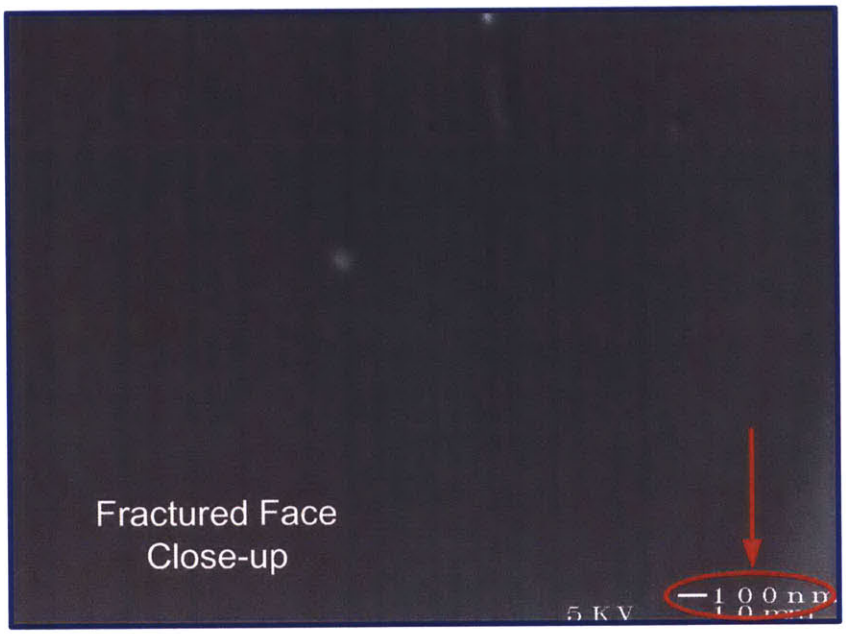
Besides lithography, FIB, and KOH, several other types of notching were considered: Reactive Ion Etching (RIE), spark machining, and hydrogen implantation. As discussed in the following sections, all were ultimately deemed unworkable.

2.4.1 Reactive Ion Etching (RIE)

Another possible way to notch specimens would be to etch a narrow trench with conventional methods, RIE most likely, and then attempt to sharpen the trench by growing a thermal oxide and then stripping the oxide [90] as is done with Atomic

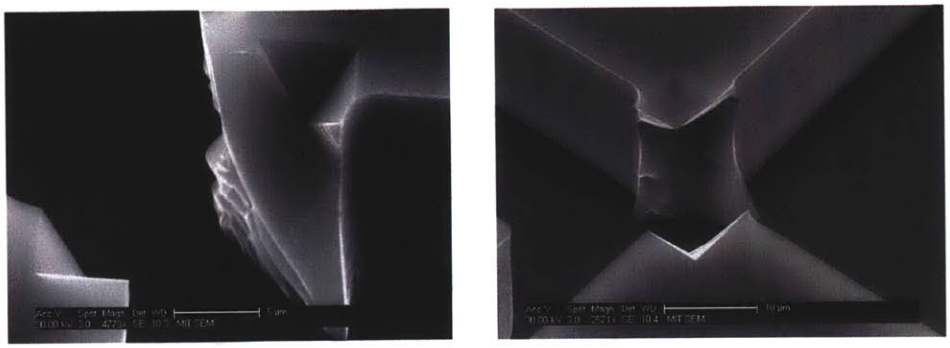


(a)



(b)

Figure 2-31: High resolution SEM images of a fractured 10 μm square specimen with a full KOH notch. Note how the rough hackled area far from the notch present in the 20 μm specimens (Figure 2-18) has been effectively removed by using a thinner specimen.



(a) One of the better pyramid notched (100) specimens

(b) A more typical pyramid notched (100) specimen

Figure 2-32: Pyramid notched (100) specimens. Note the smooth specimen sidewall.

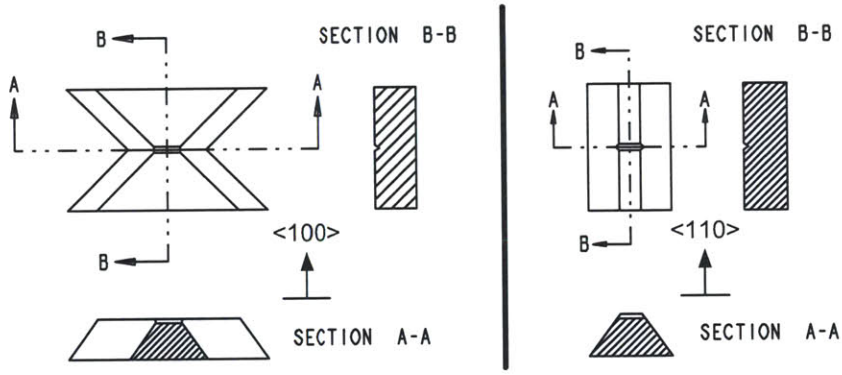


Figure 2-33: Specimens with KOH sidewalls at two different orientations. The anisotropy that generates the smooth sidewalls limits the geometry that can be achieved.

Force Microscope (AFM) tips. Some attempt would have been made to try this experimentally, if the literature did not strongly suggest that trenches tended to be blunted rather than sharpened [91, p. 1280].

2.4.2 Spark Machining

Still another potential notching technique is spark machining [13]. Like the FIB, it would be a serial process, but unlike the FIB, it is known to produce notches aligned to the crystal planes, much like KOH etching. Unfortunately, it produces not a single notch, but many; the process cannot be controlled well enough to create the notches required here.

2.4.3 Hydrogen Implantation

Hydrogen implantation [7, 9], which has seen commercial success as part of the Smart-Cut© process for making SOI wafers, was also considered for fabrication of stress concentrating notches or the surfaces themselves. In the Smart-Cut process, hydrogen nuclei, protons, are implanted in a donor silicon wafer through a layer of oxide, and the donor wafer is bonded to a handle wafer, oxide side down. At the maximum hydrogen concentration depth, the ions form platelets about 10 nm large and 1–2 atoms thick. During annealing, these platelets coalesce into hydrogen filled microcavities, the pressure in which causes splitting and cracking, leaving a thin piece of the donor wafer bonded to the handle wafer. After a touch polishing to remove approximately 10 nm of material, the SOI wafer is complete.

Hydrogen implantation is unsuitable for notching because, unlike the Smart-Cut process where the entire wafer surface is implanted, a notch implant would require in-plane patterning at nanometer scale, where masking is extremely problematic. And even if the masking difficulties could be overcome, the platelets (which are smaller than the microcavities that would actually form the notch) are 10 nm in size, the same size as the notches already created with much greater ease using the FIB.

Hydrogen implantation was also deemed unsuitable for fabricating the surfaces directly; wafers produced by the Smart-Cut process must be polished to reduce the "native" 5–11 nm RMS surface roughness [7], and the cavities formed by the implant would almost certainly preclude complementarity. Producing any surfaces at all would be very challenging, for it would require implanting at a constant concentration for the entire height of the surfaces starting from the surface of the wafer (Figure 2-34). One could imagine a device with surfaces parallel to the wafer surface rather than normal to it, but such a device would be quite different from those envisioned here and would likely suffer greatly from stiction.

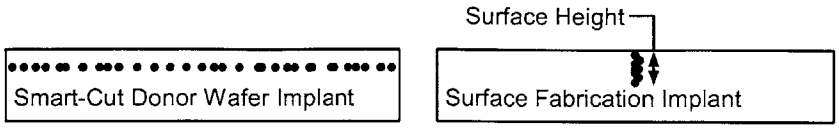


Figure 2-34: Comparison of the implants for the Smart-Cut process and for a hypothetical process to produce surfaces normal to the wafer surface. The Smart-Cut type implant is much more conventional.

2.5 Fracture Fabrication Force

The force necessary to fracture the specimens was determined with several different methods, with the goal of evaluating the feasibility of using an integrated actuator to fracture the specimens.

2.5.1 Friction Measurement

The force to fracture a 20 μm specimen fully notched with KOH was initially estimated with a friction test. The coefficient of friction between the petri dish holding the specimens and the steel translation stage of the microscope was measured by finding the incline angle at which a petri dish started to slide when placed on a similar piece of steel and found to have a maximum value of 0.58. After weighing the petri dish (and the water in it), the maximum force that can be applied to the dish before it slips was found to be 260 mN. As the dish does not slip when fracturing the specimen, this is an upper limit for the force required.

2.5.2 Flextester

The Flextester [116] (Figure 2-35) was also used to measure the force necessary to fracture a fully notched 20 μm specimen. An average force of 320 mN was required. The difference between this measurement and the friction estimate is the result of dragging the probe tip across the handle layer of the specimen while breaking the specimen in the device layer of the SOI.

Poor probe height control was a problem discussed the section 2.1.2. The ability to "feel" with the Flextester probe is even worse than it is with the more nimble

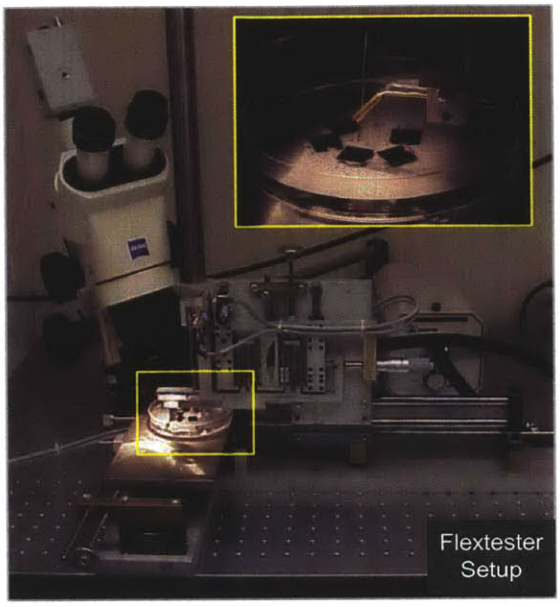


Figure 2-35: The flextester setup. A closeup view of the dies in their petri dish is inset.

standard probes, as is the optical access, so it is likely the probe is being plunged too far down, resulting in dragging and a "stubbed toe" effect that increases the measured force.

2.5.3 Analytical Calculation – FIB Notch

The fracture force of the FIB notched specimens was calculated with the expression for the stress intensity factor of a single edge cracked plate tension specimen from

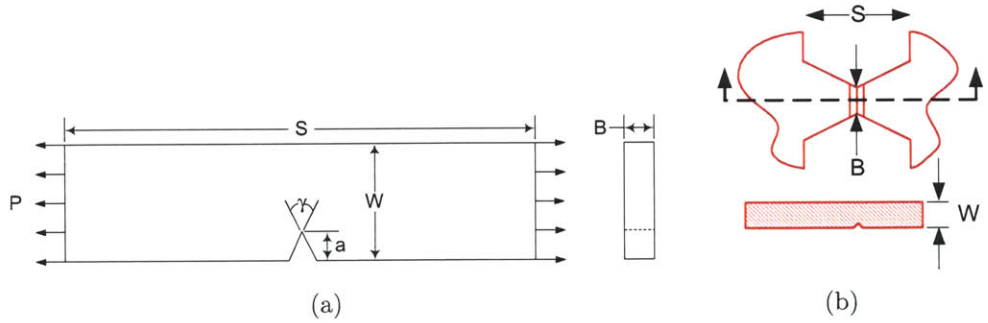


Figure 2-36: Variable definitions for use in Equation 2.7 to determine the stress intensity factor for notched specimens.

	FIB		KOH	
Specimen Width - B	**100**	**110**	**100**	**110**
10 μm	45 mN	43 mN	25 mN	24 mN
20 μm	95 mN	90 mN	59 mN	56 mN

Table 2.2: Calculated fracture force values for various specimen orientations and notch types

[20] found in [121] and [105]. The fracture force, P_c, is:

$$P_c = \frac{K_{Ic} B W}{F_I(\alpha)\sqrt{\pi a}}, \tag{2.5}$$

where

$$F_I = 1.12 - 0.231\alpha + 10.55\alpha^2 - 21.72\alpha^3 + 30.39\alpha^4, \tag{2.6}$$

$\alpha = \frac{a}{W}$, and the other variables are as defined in Figure 2-36, except that a represents the FIB depth (in this case 1 μm) rather than the notch depth. Values for silicon's critical stress intensity factors are taken from Chen and Leipold [29].

Typical values for S, W, and B are 60 μm, 10–20 μm, and 10 μm respectively. The corresponding range of values for α of 0.1 0.05 minimizes the impact of $\frac{S}{W}$ [121, p. 85, Figure 55]. The first half of Table 2.2 summarizes the results for various specimen orientations and thicknesses.

2.5.4 Analytical Calculation – Full KOH Notch

The fracture force for the KOH notched specimens was estimated analytically with Baratta's formulations for the stress intensity factors of notches [10]. Baratta's expression for the stress intensity factor, K_I, is:

$$\frac{K_I B\sqrt{W}}{P} \simeq \left\{ \left(\frac{1}{1-\frac{a}{W}} + \frac{\ln\left(1-\frac{a}{W}\right)}{\frac{a}{W}} \right) \tan\frac{\gamma}{2} + \frac{a}{W}\left[Y_{1a}\right]^2 \right\}^{\frac{1}{2}} \tag{2.7}$$

Where B is the width of the specimen, W is thickness of the specimen, i.e. the

thickness of the device layer, P is the applied tensile load, a is the depth of the notch, γ is the angle of the notch, 70.6° for KOH notches (Figure 2-36), and Y_{1a} is a function of $\frac{S}{W}$ and $\frac{a}{W}$, where S is the length of the specimen. After assuming infinite specimen length, i.e. $\frac{S}{W} = \infty$, it reduces to

$$Y_{1a}\left(\infty, \frac{a}{W}\right) = 1.99 - 0.41\left(\frac{a}{W}\right) + 18.70\left(\frac{a}{W}\right)^2 - 38.48\left(\frac{a}{W}\right)^3 + 53.85\left(\frac{a}{W}\right)^4 \quad (2.8)$$

when $0 \leq \frac{a}{W} \leq 0.6$. Results for specimens with a KOH notch 3 μm wide are in the second half of Table 2.2.

Some significant simplifications were made for the purposes of these calculations. Aside from using the fracture toughness of the the appropriate plane, the anisotropy of the silicon was neglected. The geometry of the specimen was also simplified. Its length to thickness ratio of (3–6) was assumed to be infinite and the specimen was straightened, eliminating the lithographic hourglass shape. Finally, the KOH notch itself is not perfectly sharp. Hantschel and Vandervorst found the radius of curvature at the bottom of the trench to be 5 nm [50], but it is possible they were simply measuring the curvature of their AFM tip.

2.6 Summary

A process for fabricating precision fracture surfaces has been developed. The importance of notching, surrounding structure, specimen orientation, and specimen thickness was evaluated. Smooth, planar surfaces were produced by a combination of FIB notching and a structure designed to apply pure tension to a 10 x 20 μm (110) specimen. Complementary, planar surfaces normal to the wafer plane were produced by a fully KOH notching the specimen rather that employing the FIB. Those complementary results can be converted to smooth planar surfaces by employing a square 10 μm specimen.

Various other notching techniques including RIE, hydrogen implantation, and

spark machining were explored, but found to be unsuitable. With an eye towards fracturing the specimens with an integrated actuator, the force necessary to create the surfaces was also determined both analytically and experimentally.

Chapter 3

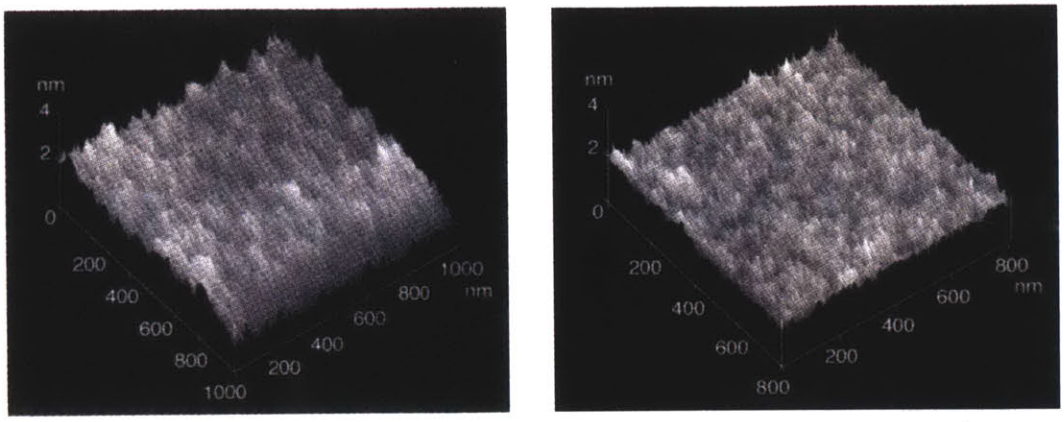
Stress Corrosion Cracking and Anisotropic Etching

In addition to the fast, brittle fracture process discussed in Chapter 2, stress corrosion cracking and anisotropic etching were studied to determine their suitability for the creation of precision surfaces. This chapter features a discussion of both, with an emphasis on their advantages and disadvantages.

3.1 Stress Corrosion Cracking

Stress corrosion cracking is a stress activated chemical corrosion process [145, 120], to which silicon is susceptible [101]. To fracture in this manner, a specimen is stressed to a large fraction of its fracture strength in a humid ambient. Cyclic loading is often employed, but is not necessary [39].

The fracture surfaces of cantilever beams fractured by stress corrosion cracking with an Atomic Force Microscope (AFM) have a surface roughness of 0.12 nm [98] (Figure 3-1(b)). The superior surface finish, which is equivalent to that of a polished wafer surface (Figure 3-1(a)), comes from the very slow propagation of the crack [5]. Unlike the fast fracture process, stress corrosion cracking is unaffected by crystal orientation. The complementarity of stress corrosion cracked surfaces is unknown, but is expected to be good because so little material is consumed during the cracking



(a) Polished surface

(b) Stress corrosion cracked surface

Figure 3-1: AFM images of polished and stress corrosion cracked surfaces from [98]

process.

A concept device for the creation of stress corrosion cracked surfaces is in Figure 3-2. The specimen is embedded within a structure very similar to the two-stage device described in Section 2.2. Instead of a pull-ring, the input stage, is attached to a spring. The other end of the spring is connected to a ratcheting folded leg flexure. The specimen is loaded by stretching the spring with the ratchet. The spring is designed to appropriately load the specimen while not itself breaking.

Like the two-stage device, this stress corrosion cracking device is fabricated by a KOH etch to define the notch, a deep reactive ion etch for the structure, and finally an HF release. Unfortunately, the device's large size, approximately 11.7 mm by 8.5 mm, makes it extremely prone to stiction. Despite arresting the release etch by dilution and never exposing the device to air, it became permanently stuck down to the handle layer, and no experiments could be done.

It would be tempting to relieve the handle layer beneath the suspended device layer structure, as in the variable capacitor fabrication process, Chapter 5 and Appendix A.5, but the large extent of the structure is again a problem. Fabricating the 1.5 mm wide relief for the capacitor device was a substantial challenge because of the difficulties depositing resist on the resulting membranes. A relief large enough for the stress corrosion cracking device could be impossible.

There are alternatives to the spring for loading the specimen, but a more serious

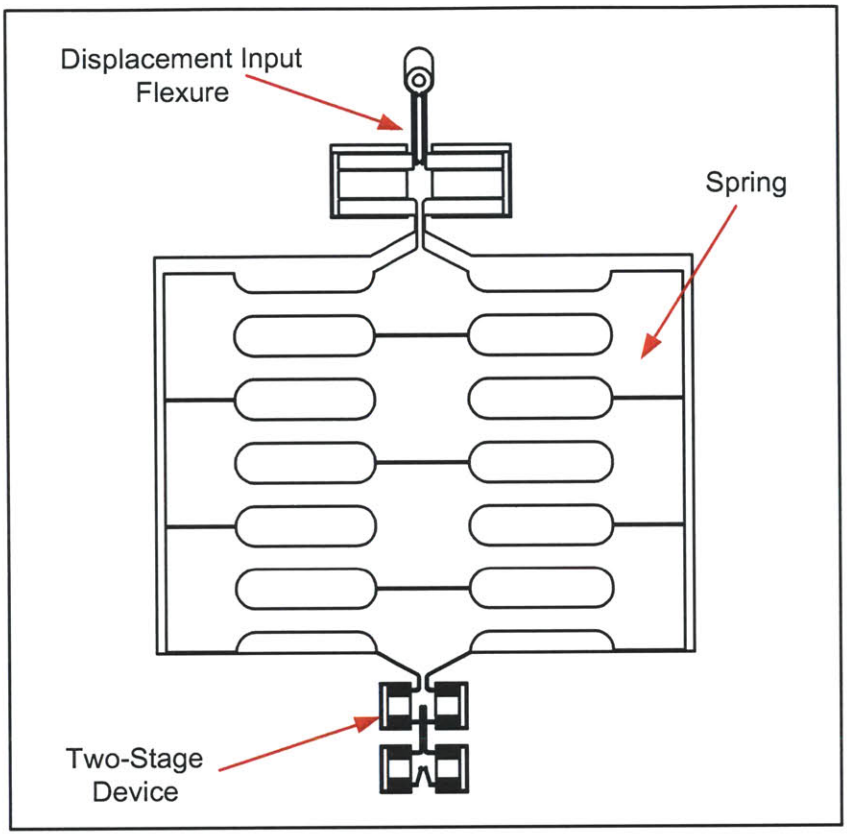
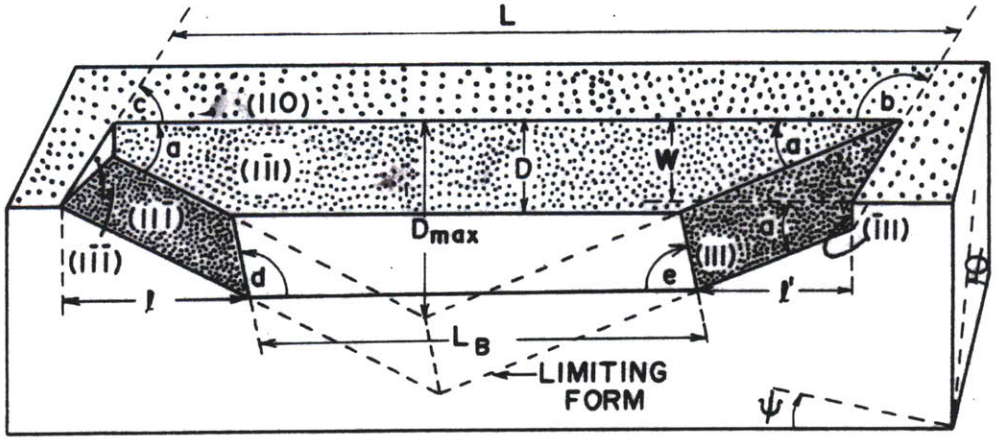


Figure 3-2: Concept device for stress corrosion cracking of silicon. The spring is stretched between the specimen and a ratcheting flexure.

problem is the difficulty of stress corrosion cracking an entire specimen. As the stress corrosion crackfront advances, the stress intensity factor, K_I, of the specimen also increases. The crack will eventually advance far enough that the critical stress intensity factor, K_{Ic}, is reached. At that point, fast fracture will occur. As the results for Chapter 2 have shown, this is not necessarily bad, but is hardly a fitting return for all the effort necessary to initiate a stress corrosion crack.

3.2 Anisotropic Etching

In Chapter 2, stress concentrating notches are anisotropically etched with potassium hydroxide (KOH) into (100) silicon wafers. Because the etch rate of (111) planes is very slow, those etches produced self-terminating inverted pyramid-like structures



$$
\begin{array}{lll}
a = 30^\circ & d = 125.26^\circ & D = \frac{L}{2\sqrt{3}} \\
b = 109.5^\circ & e = 54.74^\circ & \ell = \sqrt{3}D \\
c = 70.5^\circ & L_B = L - 2\sqrt{3}D + \frac{3\sqrt{2}W}{4} & \ell' = \sqrt{3}D - \frac{3\sqrt{2}W}{4}
\end{array}
\tag{3.1}
$$

Figure 3-3: "The geometry of the slow etching {111} planes that develop in a long narrow groove etched into the {110} surface of silicon" [71] when etched with KOH. The angles denoting mis-orientation from the principal crystal axes, Ψ, Φ, and θ are zero.

(Figure 2-23). If a (110) wafer had been used instead, a vertical-walled trench like that in Figure 3-3 would have been produced instead [73, 71, 67, 72, 74]. The vertical sidewalls of the trench are extremely smooth (111) planes.

Figure 3-4 is an AFM image of some anisotropically etched (111) planes. The surface roughness of less than 0.4 nm rivals the 0.12 nm surface roughness of finely polished silicon surfaces. The surfaces in the figure are not normal to the wafer plane and did not form trenches because they were fabricated with a process designed to produce X-ray diffraction gratings [28, 44]. Among other special features, that process employs wafers cut off-axis to produce extremely smooth grating-like structures.

As a test, trenches with sidewalls roughly equivalent in size to the fracture surfaces in Chapter 2 were etched in a (110) wafer using the expressions in Equation 3.1 to size the mask openings. The high quality sidewalls produced by the etch can be seen in Figure 3-5. There were some problems with contaminants, but the vast majority of the particles were dissolved with a hydrochloric acid (HCl) solution following the procedure in [109]. A more thorough post-etch rinse would likely prevent such

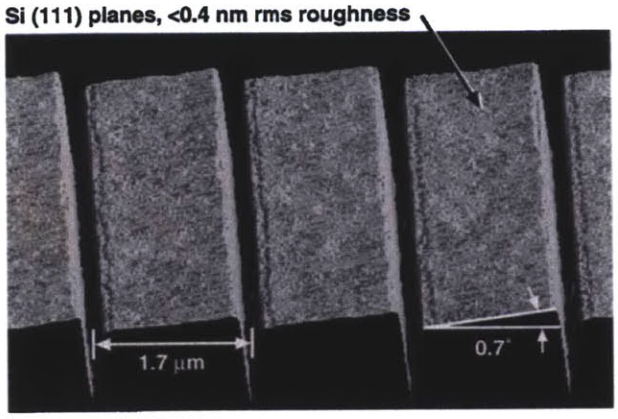


Figure 3-4: AFM image of anisotropically etched (111) planes from [44]. Note the remarkable surface roughness of less than 0.4 nm.

contamination altogether. Angular misalignment of the mask with respect to the underlying crystal structure is an issue, but rather than employing specialized alignment features [78, 141] and its attendant etch, the trenches were simply over-etched by approximately 200%.

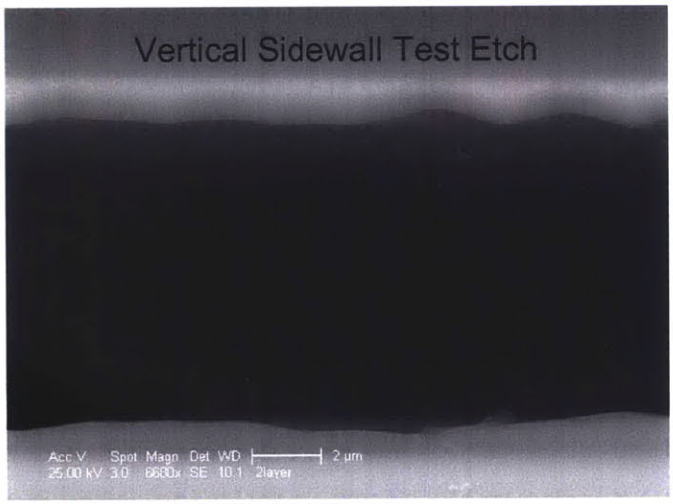


Figure 3-5: (111) sidewall of a trench etched to compare the results of anisotropic etching with fracture fabrication.

To fabricate a device equivalent to the variable capacitor in Chapters 4 and 5 with anisotropically etched rather than fracture fabricated surfaces, SOI wafers with (110) device layers could be used, with the trench etches stoping on the buried oxide. A nested mask [65] may be necessary to properly protect the anisotropically etched

surfaces during the DRIE, but the biggest problem is likely to be the normally-open nature of the device.

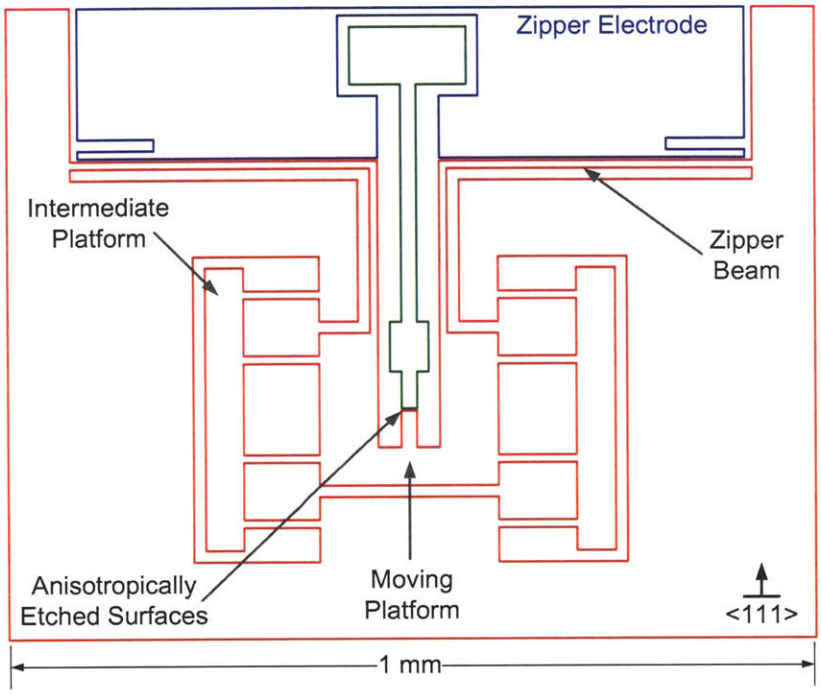


Figure 3-6: Concept for a variable capacitor with anisotropically etched surfaces as separable parallel plates.

Anisotropically etched (111) planes have very low surface roughness and are by their nature very parallel, but their proximity is limited by lithographic technology, and is therefore likely to be in the single micron range. Minimizing the error motions of the compliant mechanism supporting the surfaces is critical if their minimum separation is to be determined by their geometry rather than deviations from true introduced by the flexure. The concept in Figure 3-6 achieves that precision by minimizing the size of the device. Because the flexure no longer needs to refine an externally applied load or to withstand the trauma of fracture, it can be much smaller than the device in Figure 4-25. Reducing the structure's size reduces its vulnerability to error motions from residual stress; residual stress typically results in undesired curvature, which in turn produces an angular or Abbe error [129]. A smaller structure has a smaller lever arm, and therefore less gain for the Abbe error.

The electrostatic zipping actuator of the concept device in Figure 3-6 features a anisotropically etched zipper. Though the geometry could also be created with DRIE, using anisotropic wet etching instead would be considerably less expensive and has the potential to produce atomically smooth scallop free surfaces. Wet etching the zipper limits the stroke of the device because the electrodes must be straight, but a maximum stroke equivalent only to the minimum lithographic linewidth is required for this device; any additional stroke would be useless as the etched surfaces at the center of the device would already be in contact.

Wet etching the entire device structure is a possibility, but would likely be extremely challenging. Fruhauf's process [46, 49] is not appropriate; it etches along (100) planes in (100) wafers. Others have succeeded at wet etching entire structures [75, 84, 139], especially comb drives, but the available geometry is limited because different planes in the {111} family are not perpendicular, so any corners in the device will be irregular and non-perpendicular. A combined DRIE and KOH process like [31], is an option, but is likely to be as expensive and cumbersome as the nested mask process [65] mentioned earlier.

3.3 Summary

Stress corrosion cracking produces excellent surfaces, but is impractical because the necessary hardware is too large and because producing a surface solely by stress corrosion cracking is extremely difficult. Fabricating the surfaces by anisotropic etching is an appealing possibility, but challenges in the design of the flexure and the fabrication process will have to be overcome. The flexure must be extremely linear and free of error-motions if the surfaces are not to touch at a single point prior to closing, and the fabrication challenges of integrating the anisotropically etched surfaces with all of the other necessary geometry are significant. Despite these challenges further investigation of a device built around a pair of anisotropically etched structures is appropriate, and will be discussed in Chapter 6.

Chapter 4

Variable Capacitor Analysis and Design

This chapter describes the design and analysis of a variable capacitor employing single crystal silicon fracture surfaces as the separable plates. Potential applications include RF MEMS [150], impedance spectroscopy [47], and experiments involving electric fields in extremely small gaps. Fabrication and testing of the device will be discussed in Chapter 5.

The key challenge is the stable separation of the fracture surfaces. One surface is anchored to the handle layer of the Silicon On Insulator (SOI) wafer. The other is supported by a flexural bearing. The position of the moving surface is determined by a three way force balance between the actuator, the compliance of the flexural elements, and the capacitive force of the electric field between the two fracture surfaces.

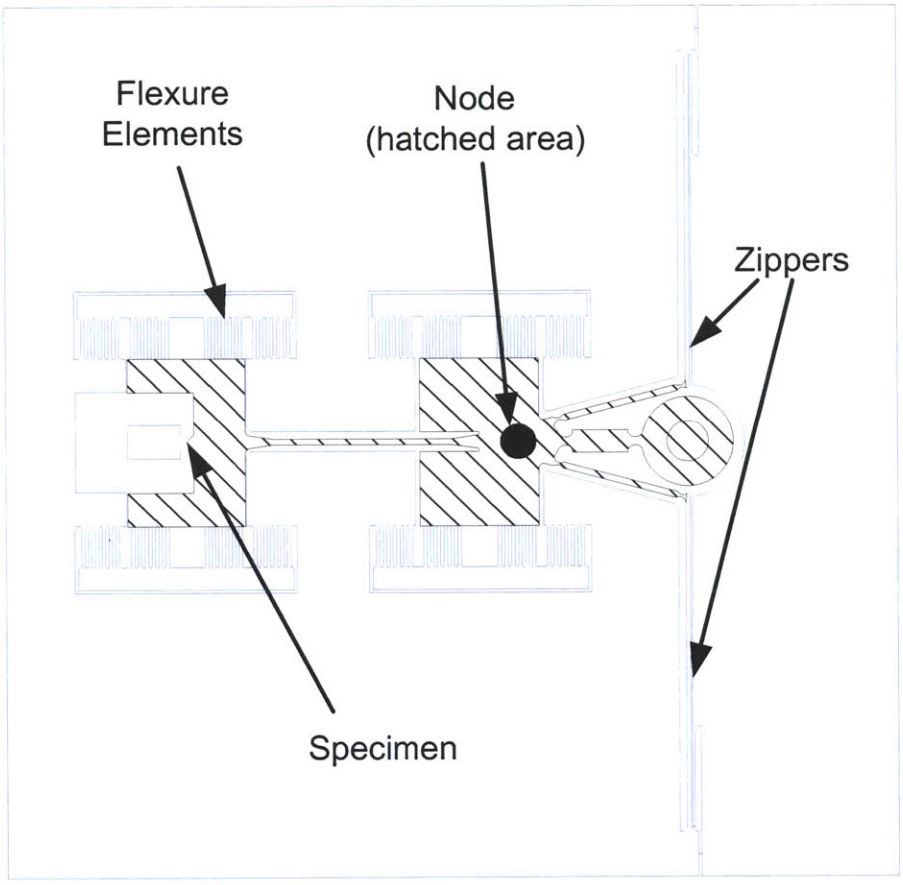
The principal advantage of fracture surfaces over etched surfaces is their flatness or complementarity. They can therefore approach each other on the nanometer scale without touching. And that when they do touch, a good seal is formed between them. Pairs of charged surfaces are famously susceptible to unstable pull-in [124]; a design where the separation of the surfaces becomes unstable before they would have touched due to their deviation from the ideal would not be making the most of the surfaces. The optimization of the design to prevent this is thus a major portion of this chapter.

The force necessary to fabricate the specimens (Section 2.5) is quite large for a MEMS device. A comb drive producing the necessary force could easily have thousands of elements, the successful microfabrication of which would be a considerable challenge in its own right. Devices for measuring the strength of polysilicon (a weaker material than single crystal silicon) are known to require startlingly large actuators [68]. A parallel plate style electrostatic actuator would be similarly large and unsuitable. A thermal actuator could produce the necessary force, but its stiffness would make examination of the surfaces problematic, and it would not be amenable to fine displacement control. A piezo actuator could combine the necessary strength and precision, but would have to be assembled with the silicon device, a significant challenge. Given these constraints, it was decided to use the actuator only for control of displacement; fracture was left to an external probe. Fracturing with a probe also minimizes deviation from the existing fracture fabrication process.

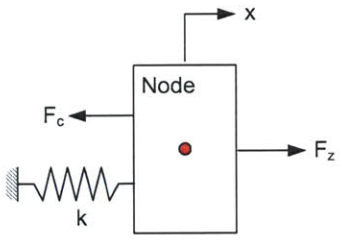
A rather limited set of applications might require an integrated fracture actuator. Single use monolithic valves [66] and systems requiring the fracture be done in vacuum are two potential examples. For applications where the fracture force can be provided externally, it is tempting to employ centrifugal force, but the numbers do not quite work. Even at a radius of 50 mm and a spin speed of 10,000 RPM, a 2 mm diameter mass disk (20 μm thick) generates only 14% of the necessary force. A more reasonable method would be to fracture a whole wafer of devices in parallel with a probe card.

4.1 Single Node Model

To minimize the risk of upsetting the established fracture process, the concept for the variable capacitor consisted of a two-stage device (Chapter 2) to which a zipper actuator was attached (Figure 4-1(a)). For the single node analysis, the variable capacitor device is reduced to a spring representing the flexure that guides the separation of two surfaces, an actuator, and the capacitor formed by the two surfaces (Figure 4-1(b)). These three forces act at a single node whose displacement is determined by equilibrium.



(a) Concept for variable capacitor device



(b) Single node lumped parameter model of variable capacitor device

Figure 4-1: Implementation of single node model for the variable capacitor

4.1.1 The Forces

The force from the flexural element is described by Hooke's Law:

$$F_k = kx. \tag{4.1}$$

The flexure spring constant, k, was determined analytically and by Finite Element Analysis (FEA), see Appendix E for a derivation of the appropriate single crystal silicon material properties. All variables are defined in the nomenclature section preceding the introduction. The displacement, x, of the surface supported by the flexure is equivalent to the surface separation and has a value of zero when the gap is completely closed.

All lengths are measured in microns and all forces in milliNewtons, with the equations modified as necessary. The separation of the surfaces is measured in microns and flexure stiffness is calculated in $\frac{\text{mN}}{\mu\text{m}}$.

As a practical matter, the gap between the surfaces is unlikely ever to be completely closed. When the surfaces are created by fracture, a native oxide forms on each face. 56% of that oxide is above the original silicon surface level [25] (Figure 4-2). This expansion results in a positive minimum achievable displacement. Ideally, the pull-in displacement would be less than this minimum displacement.

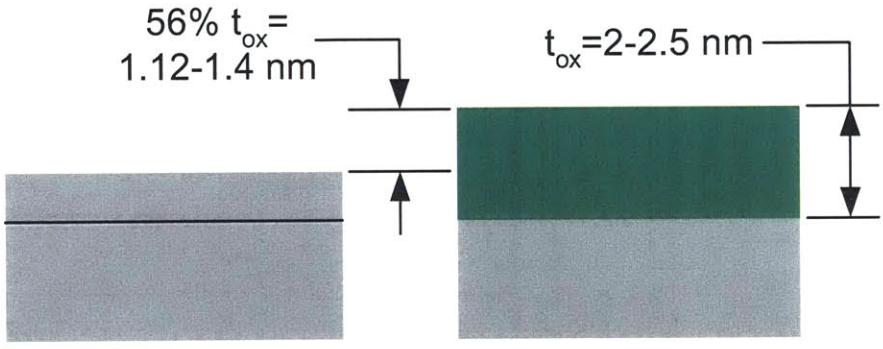


Figure 4-2: When oxide forms on a silicon surface, 56% of the oxide forms above the level of the original silicon surface.

The force from the capacitor is described by the standard parallel plate actuator

equation [124]:

$$F_c = 1000 \cdot \frac{\epsilon_0 (A \cdot 10^{-12}) {V_c}^2}{2(x \cdot 10^{-6})^2}, \tag{4.2}$$

where ϵ_0 is $8.854 \cdot 10^{-12} \frac{\mathrm{F}}{\mathrm{m}}$, A is the area of one plate – in $\mu\mathrm{m}^2$, and V_c is the potential across the plates. For simplicity, this equation will be replaced by:

$$F_c = \frac{B}{x^2}, \tag{4.3}$$

where

$$B = 1000 \cdot \frac{\epsilon_0 A {V_c}^2}{2}. \tag{4.4}$$

The equation is invalid for displacements below zero, because the two faces of the capacitor would be in mechanical contact and the sign of the electrical force becomes incorrect.

The force-displacement curve of the zipper actuator is described by the equation [81, 82]:

$$F_z = 2 \cdot \frac{Q V_z^{\frac{3}{2}} b}{\sqrt{\Delta - x + \frac{h_0}{\epsilon_r}}} \cdot \left(\frac{h}{h_0}\right)^{\frac{3}{4}}, \tag{4.5}$$

where V_z is the voltage across the zipper, b is the thickness of the zipper – in this case the thickness of the SOI device layer, Δ is the zipper stroke, h_0 is the thickness of the silicon dioxide dielectric ($0.250\,\mu\mathrm{m}$), ϵ_r is the dielectric constant of the silicon oxide (3.8), h is the height of the zipper beam, and Q is a constant ($2.72 \cdot 10^{-6}$) derived from FEA [81]. See Figure 4-3 for a graphical definition of these variables. The leading factor of 2 originates from the assumption that a symmetrical zipper with two beams will be used. Though perhaps not strictly necessary, a symmetrical zipper is less likely to generate moments.

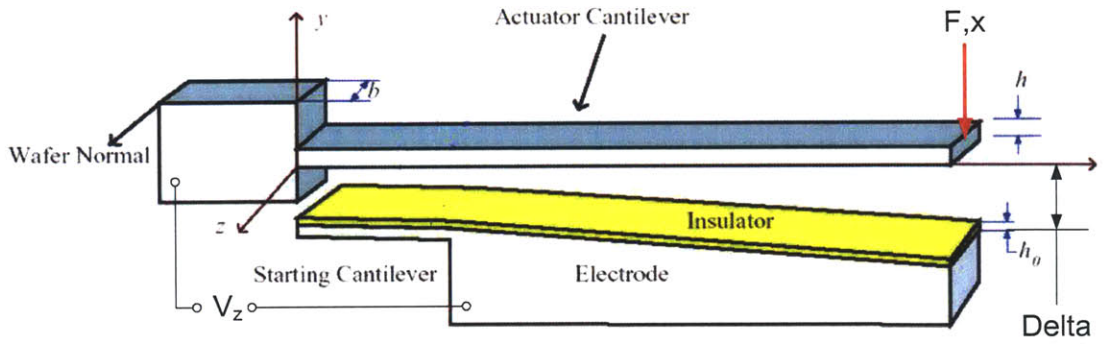


Figure 4-3: Zipper variable definitions, altered reproduction from [81]

For further manipulation, the equation is simplified to:

$$F_z = \frac{C}{\sqrt{\delta - x}}, \tag{4.6}$$

where

$$C = 2QV_z^{\frac{3}{2}} b \left(\frac{h}{h_0}\right)^{\frac{3}{4}} \tag{4.7}$$

and

$$\delta = \Delta + \frac{h_0}{\epsilon_r}. \tag{4.8}$$

Like the expression for the attractive force between the capacitor plates, Equation 4.6 is valid only for certain displacements. Specifically, displacements larger than $\Delta - 2h_0$, the maximum stroke of the zipper, are not allowed. Mechanically, the zipper would be fully closed and for displacements greater than $\Delta + \frac{h_0}{\epsilon_r}$, evaluation of Equation 4.6 produces an imaginary number.

Figure 4-4 is a plot of the force *vs.* displacement curves for the flexure, the capacitor, and the zipper at various voltages. The attractive force of the capacitor plates becomes quite large at small displacements, potentially creating a pull-in instability, whose effects should be minimized.

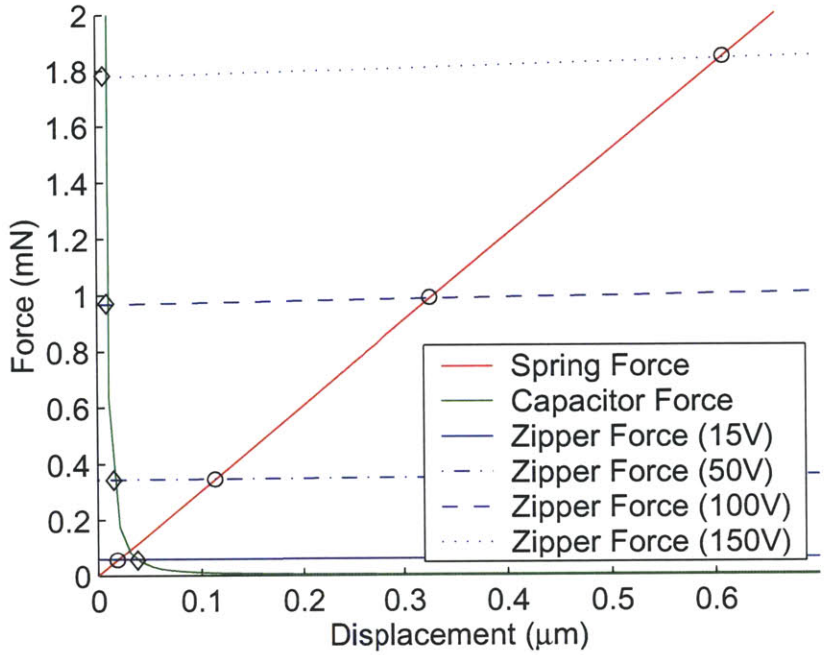


Figure 4-4: A plot of all the forces. The force from the capacitor becomes quite large at small separations.

4.1.2 Equilibrium

For equilibrium, the three forces must sum to zero:

$$0 = -F_k - F_c + F_z. \tag{4.9}$$

Substituting in the relations from the previous section:

$$0 = -kx_0 - \frac{B}{x_0^2} + \frac{C}{\sqrt{\delta - x_0}}, \tag{4.10}$$

where x_0 is an equilibrium displacement. Rearranging the equation into polynomial form yields:

$$0 = k^2 x_0^7 - k^2 \delta x_0^6 + \left(2Bk + C^2\right) x_0^4 - 2Bk\delta x_0^3 + B^2 x_0 - B^2 \delta. \tag{4.11}$$

In Figure 4-5 are plots of the five different real solutions to the equilibrium poly-

nomial and the results of substituting those roots back into the polynomial. Although the quality of the roots varies considerably with zipper voltage and solution to solution, all are of the order 10^{-11} or less. This numerical noise in the roots corresponds to a 10^{-14} mN level error in the force balance of the physical solutions.

The different root loci were assembled by sorting the roots produced at each voltage and then manually splicing the sets together at discontinuities such as when the number of real roots jumps from three to five.

Solutions A, B, and E are non-physical. A and B fall outside the range of validity of the capacitor force function (Equation 4.2). They should be interpreted as having the two capacitive plates stuck together at the minimum displacement possible – twice the thickness of the native oxide above the surface. Solution E is beyond the maximum stroke of the zipper actuator; the zipper is stuck closed.

Solution C is the small displacement solution. The zipper force and the capacitor force are balanced with very little contribution from the flexure spring force (Figure 4-6); the displacement is too small for the spring to make a significant contribution. In Figure 4-4, the force plot, Solution C is approximated by the intersection (marked with a diamond, $\diamond$) of the capacitor force line and the various zipper force lines.

Solution D is the large displacement solution. The zipper force and the spring force are balanced with very little contribution from the capacitor (Figure 4-6); the displacement is too large for the field between the fracture surfaces to make a significant contribution. Equivalent to Solution C, the solution is approximated by the intersection (marked with a circle) of the zipper force lines and the spring force line in the force plot, Figure 4-4.

A stability analysis is necessary to determine the validity of these solutions. An unstable solution is not physically realizable.

4.1.3 Stability

To assess the stability of the equilibrium points of which each solution is composed, the product of the system mass, m, and the linearized natural frequency, $\tilde{\omega}_n$ as defined in the equation [147]:

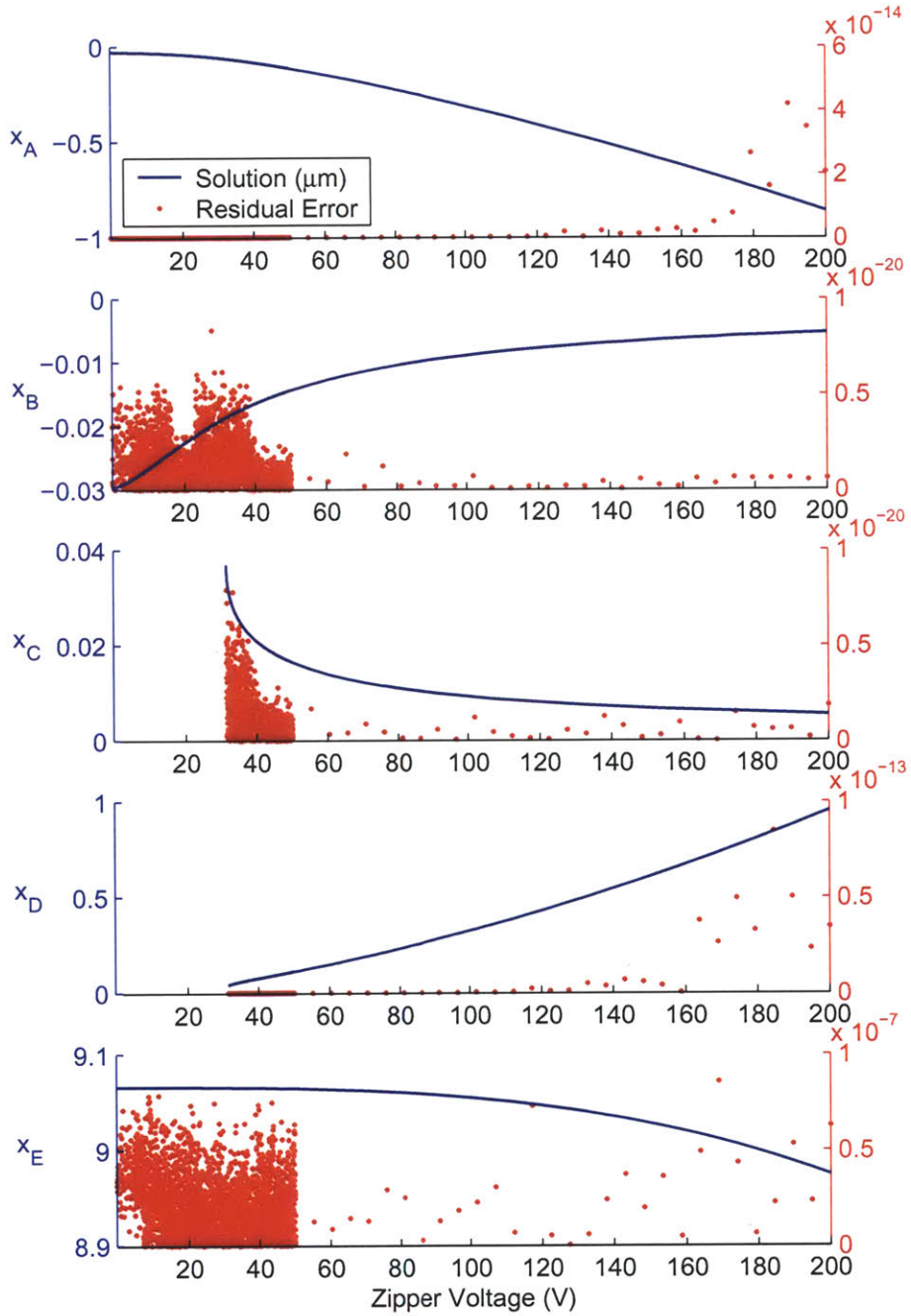


Figure 4-5: Plots of the polynomial roots and the value of the polynomial at those roots as a function of zipper voltage. To more clearly capture the behavior there, the density of the zipper voltage vector is higher at lower voltages. The numerical error in the polynomial solution corresponds to a 10^{-14} mN level error in the force balance of the physical solutions. The scale for the polynomial evaluation is on the right axis. Solutions A, B, and E are non-physical because they fall outside the range of validity for either the zipper or the capacitive force equations.

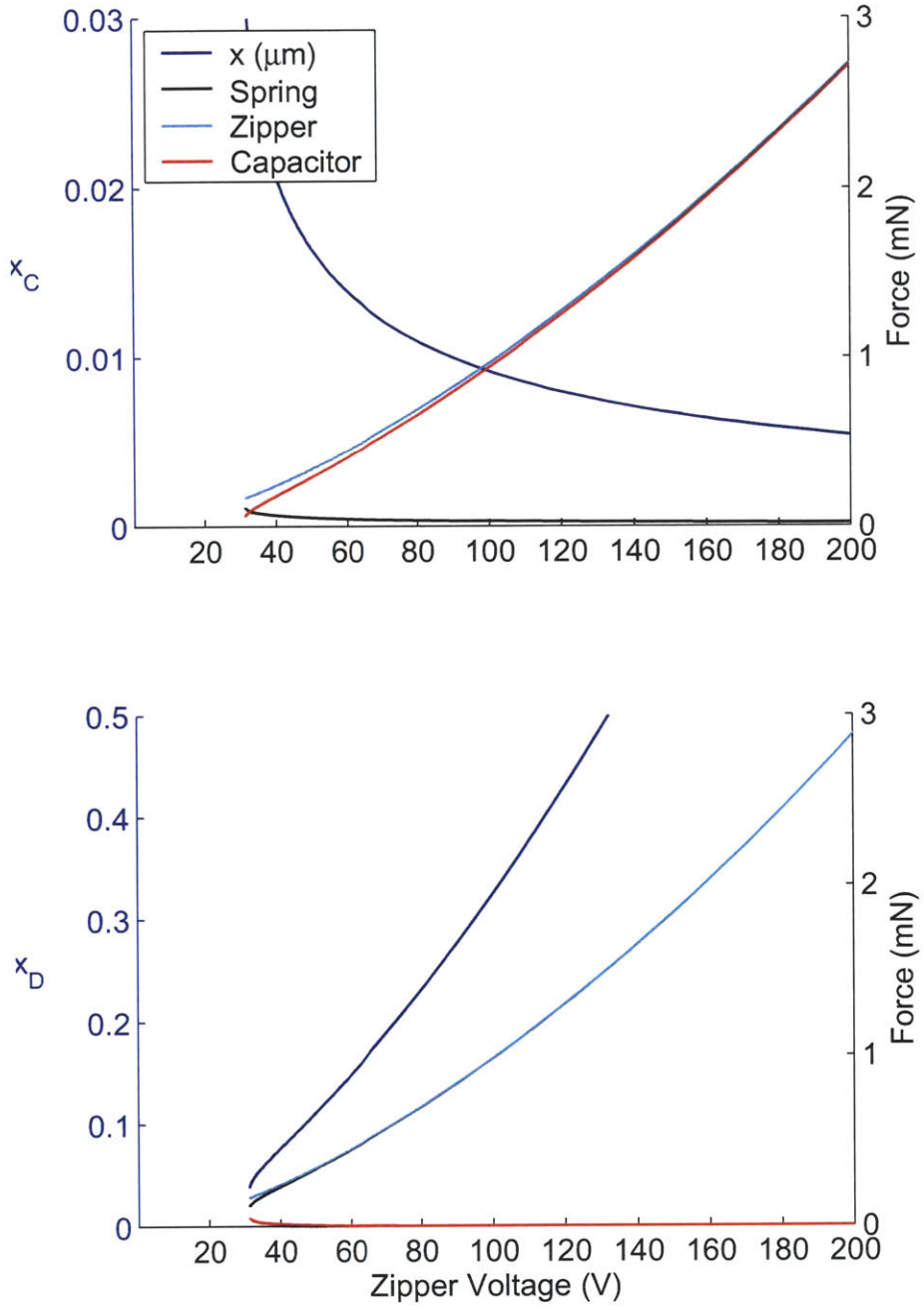


Figure 4-6: Plots of solutions C and D along with the forces from the spring, capacitor and zipper.

$$\ddot{\zeta} + \tilde{\omega}_n^2 \zeta = 0, \tag{4.12}$$

where ζ is a generalized coordinate will be calculated. If $\tilde{\omega}_n^2 > 0$, or in this case $m\tilde{\omega}_n^2 > 0$ (mass is assumed to always be positive), the equilibrium point is stable.

For a small disturbance, x, about the equilibrium point, x_0, the equation of motion (based on Equation 4.10) is:

$$(x_0 \ddot{+} x) + \frac{k}{m}(x_0 + x) + \frac{B}{m(x_0 + x)^2} - \frac{C}{m\sqrt{\delta - x_0 - x}} = 0. \tag{4.13}$$

Since $\ddot{x}_0 = 0$,

$$\ddot{x} + \frac{k}{m}x_0 + \frac{k}{m}x + T_1(x_0 + x) - T_2(x_0 + x) = 0 \tag{4.14}$$

where

$$\begin{aligned} T_1(x_0 + x) &= \frac{B}{m(x_0 + x)^2} \\ &\approx T_1(x = 0) + x \left.\frac{\mathrm{d}T_1}{\mathrm{d}x}\right|_{x=0} \\ &\approx \frac{B}{mx_0^2} - \frac{2Bx}{mx_0^3} \end{aligned} \tag{4.15}$$

and

$$\begin{aligned} T_2(x_0 + x) &= \frac{C}{m\sqrt{\delta - x_0 - x}} \\ &\approx T_2(x = 0) + x \left.\frac{\mathrm{d}T_2}{\mathrm{d}x}\right|_{x=0} \\ &\approx \frac{C}{m\sqrt{\delta - x_0}} + \frac{Cx}{2m(\delta - x_0)^{\frac{3}{2}}} \end{aligned} \tag{4.16}$$

Recombining the results from the linearizations in Equations 4.15 and 4.16 with

Equation 4.14 yields

$$\ddot{x} + \frac{k}{m}x_0 + \frac{k}{m}x + \frac{B}{mx_0^2} - \frac{2Bx}{mx_0^3} - \frac{C}{m\sqrt{\delta - x_0}} - \frac{C}{2m\left(\delta - x_0\right)^{\frac{3}{2}}} = 0, \tag{4.17}$$

which upon subtraction of the equilibrium equation (Equation 4.10) produces

$$\ddot{x} + x\left(\frac{k}{m} - \frac{2B}{mx_0^3} - \frac{C}{2m\left(\delta - x_0\right)^{\frac{3}{2}}}\right) = 0. \tag{4.18}$$

Thus,

$$m\tilde{\omega}_n^2 = k - \frac{2B}{x_0^3} - \frac{C}{2\left(\delta - x_0\right)^{\frac{3}{2}}}, \tag{4.19}$$

an expression readily evaluated numerically. An analysis with Lyapunov's direct method would give an idea of each equilibrium point's radius of attraction, but this indirect analysis should be sufficient and is more easily reduced to a program.

Strictly, $m\tilde{\omega}_n^2 > 0$ guarantees only stable oscillation. Damping has not been included in this model, but it will be present, and likely be large, due to the mechanical rubbing and squeeze film damping inherent to the zipper design. Any stable oscillation will quickly be damped out.

In Figure 4-7 is a pair of plots of the two different physical solutions to the equilibrium polynomial (Equation 4.11) and the $m\tilde{\omega}_n^2$ product for each solution at each zipper voltage. Solution C is unstable over the whole voltage range, but most closely approaches stability near its inception at approximately 30 V, while Solution D is stable over the whole range, but most closely approaches instability near its inception. When starting on Solution D with a large displacement and actuation voltage, one could imagine displacement reducing as the voltage is turned down until a critical point is reached. Below that critical voltage and displacement, Solution C is valid, but unstable, and the separation of the surfaces collapses.

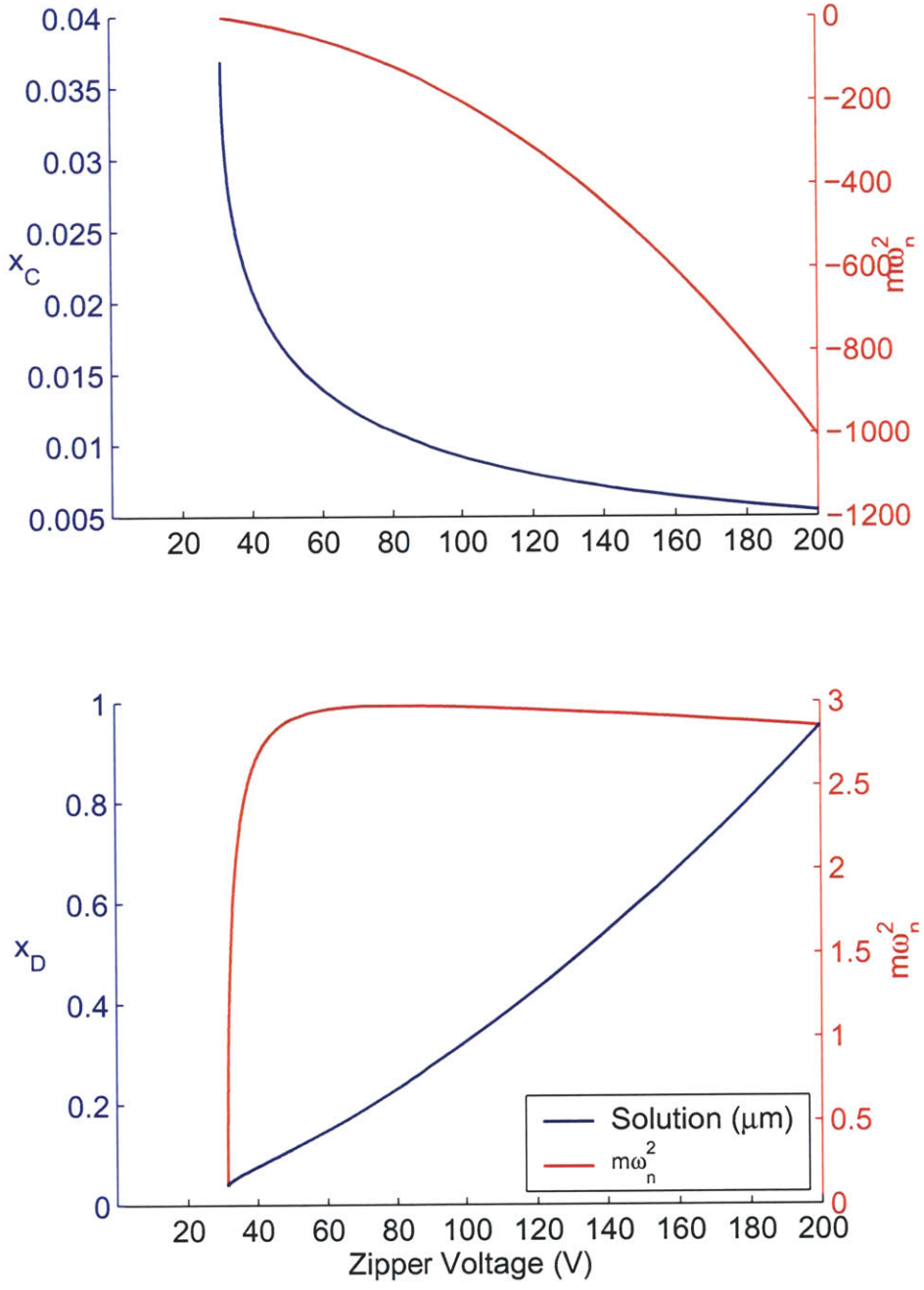


Figure 4-7: Plots of Solutions C and D and the mass-linearized natural frequency squared product ($m\tilde{\omega}_n^2$), an indicator of local stability.

4.1.4 Capacitance

The minimum stable gap coincides with the maximum capacitance the device can achieve. At smaller gaps that could produce larger capacitances, the plate separation is unstable and is really zero. And when the gap is closed, only a very small potential can be sustained between the surfaces before their thin native oxide breaks down.

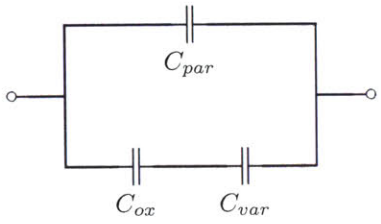


Figure 4-8: Circuit model of the device capacitances.

The capacitance of the device is represented by the lumped model in Figure 4-8. The parasitic capacitance, C_{par}, is in parallel with the capacitance of the gap, which is itself a serial combination of the capacitance due to the native oxide on the fracture surfaces, C_{ox}, and the variable capacitance, C_{var}, between the surfaces. The combined capacitance is:

$$C_{device} = C_{par} + \frac{C_{ox}C_{var}}{C_{ox} + C_{var}} = C_{par} + \frac{\epsilon_r \epsilon_0^2 A}{\epsilon_0 t_{ox} + \epsilon_r \epsilon_0 t_{var}}, \tag{4.20}$$

where ϵ_r is the dielectric constant of silicon oxide, 3.8, t_{ox} is the combined thickness of the oxide on both faces, and t_{var} is surface separation, x_D. The capacitances have been combined using the standard formulas for parallel and series impedances. C_{var} and C_{ox} have been evaluated with the expression for the capacitance of parallel plates:

$$C_{ox} = \frac{\epsilon_r \epsilon_0 A}{t_{ox}}, \quad C_{var} = \frac{\epsilon_0 A}{t_{var}}. \tag{4.21}$$

The parasitic capacitance was estimated with an ANSYS model of the device (Appendix C). The model (Figure 4-9) consists of the specimen anchor, a portion of the flexure, a portion of the handle layer, the oxide beneath the specimen anchor, and the air surrounding the device. The extent of the flexure, handle layer, and

air modelled was experimented with to confirm that adding more of each did not substantially affect the result. The principal source of the parasitics, 0.9 pF, is the capacitor formed between the specimen anchor and the handle layer, with the buried oxide serving as a dielectric. Compared to that, the 7 fF between the specimen anchor and the flexure is negligible.

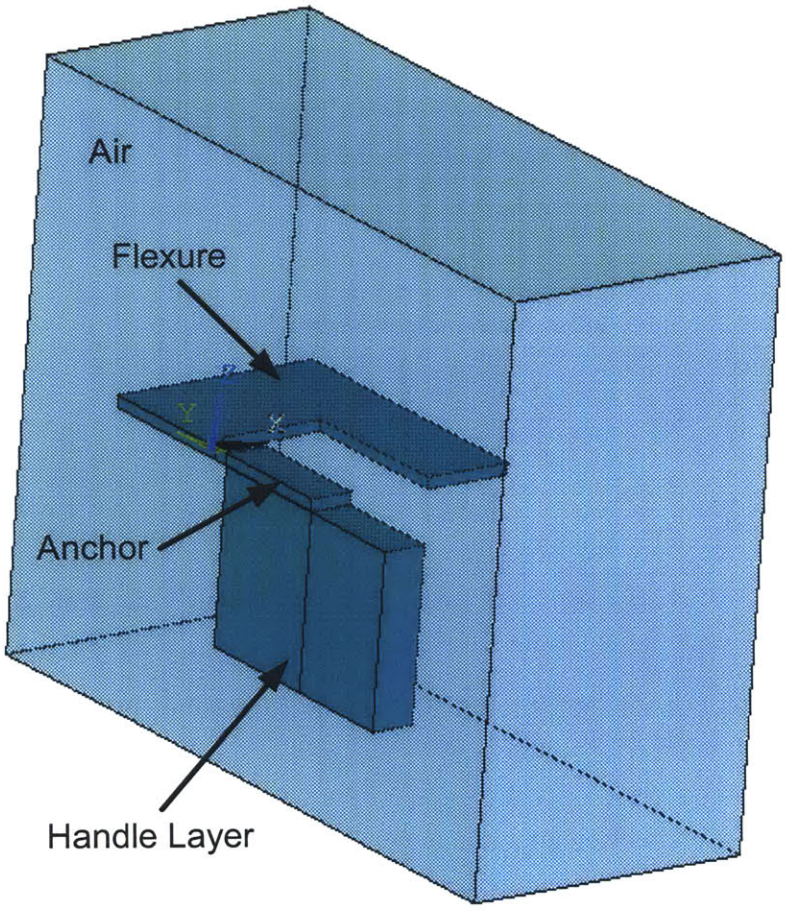


Figure 4-9: ANSYS model of the variable capacitor device. The dominant capacitance is that between the specimen anchor and the handle layer. Only half the device was modelled (and the resulting capacitance numbers doubled) to enable the construction of a more densely meshed model; the academic software license is node-limited.

The plot in Figure 4-10 of the device capacitance with respect to fracture surface separation illustrates the importance of minimizing the surfaces' minimum stable separation; the majority of the capacitance change comes below 50 nm, and by 200 nm,

the variable capacitance between the surfaces (C_{var}) is essentially zero, and the device capacitance is equal to the parasitic capacitance. Setting aside issues related to experimental convenience (e.g. being able to see the device move with a microscope), a design tradeoff that reduced the minimum stable gap at the expense of reducing the maximum stroke of the device would be a good one; the lost stroke would not materially reduce the device' capacitance range.

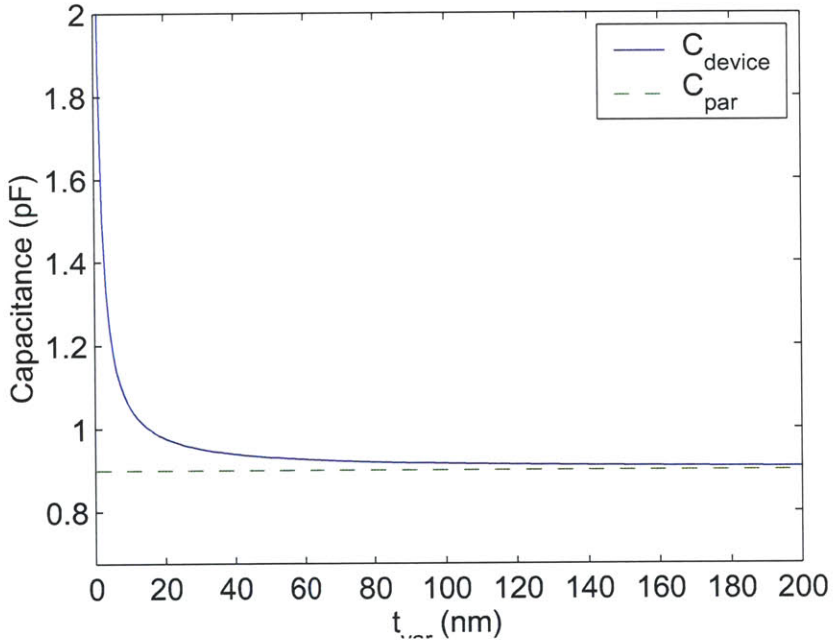


Figure 4-10: A plot of the device capacitance (C_{device}) with respect to fracture surface separation (t_{var}) based on Equation 4.20

The size of the parasitic capacitor formed by the specimen anchor scales directly with the anchor's area, so the anchor was made as small as possible. Provision was also made to drive the handle layer as a shield, but all capacitive calculations were made with with the assumption that the capacitance would not be shielded.

4.2 Discussion

When plotted together in Figure 4-11, it is clear the two solutions are in some sense continuous. For better device performance, i.e. a smaller pull-in displacement, it is

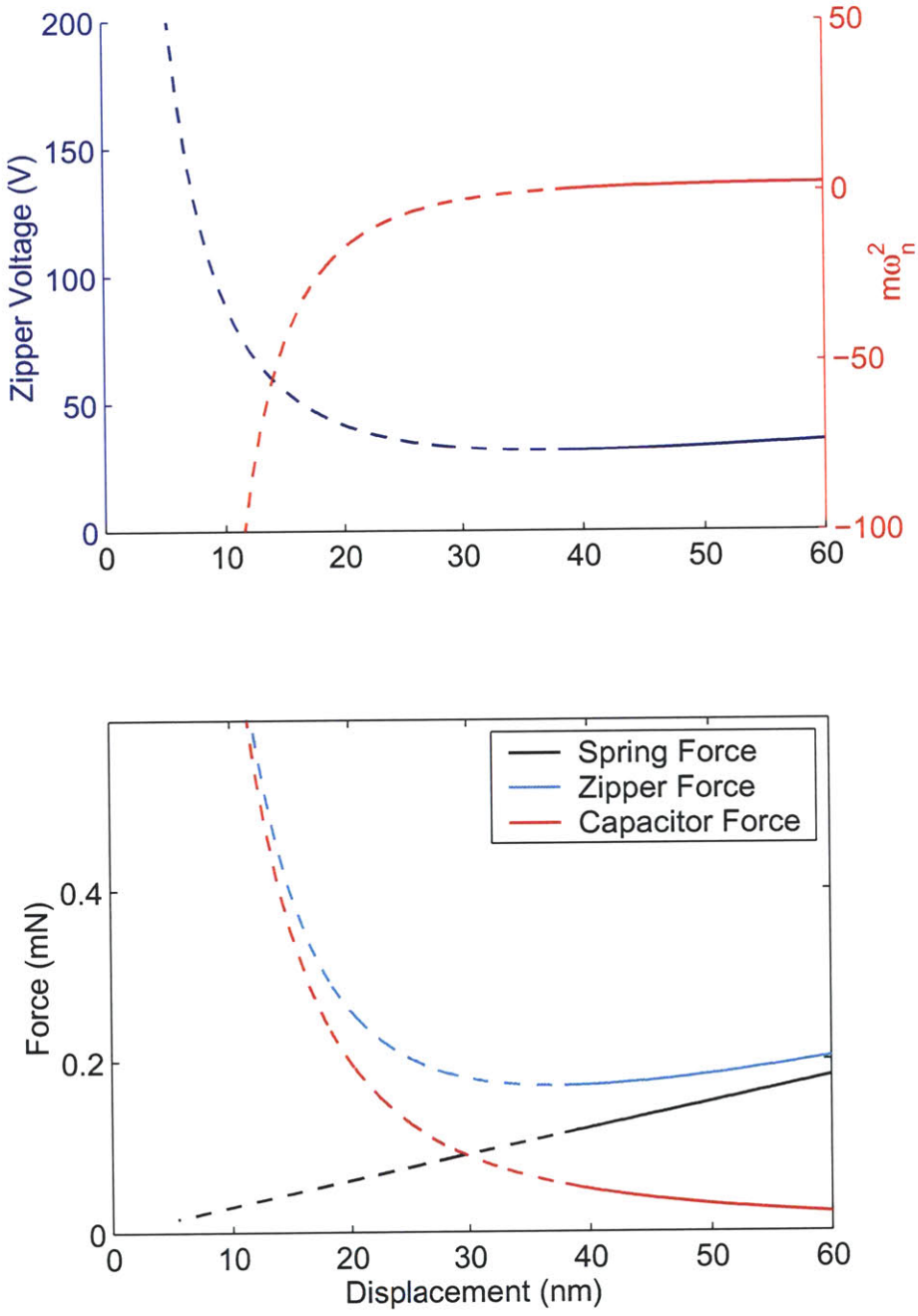


Figure 4-11: Solution C (dashed) and Solution D plotted on the same graph. Note the continuous transition from Solution D (stable) to Solution C (unstable).

necessary only to shift the point at which the transition from Solution D, the stable solution, to Solution C, the unstable solution, occurs. Figure 4-6 and the lower panel of Figure 4-11 suggest this might be done by stiffening the flexure spring or by adding a constant opening force (perhaps from an independently driven comb drive) to make the spring-zipper equilibrium represented by Solution D dominant at smaller displacements.

4.2.1 Stiffened Flexure Spring

Increasing the stiffness of the flexure by a factor of ten decreases the pull-in displacement substantially (Figure 4-12). The principal downside is a commensurate reduction in the maximum stroke; the same actuator force separates the surfaces by a factor of ten less. From an electrical point of view, the consequences are less severe, however. The capacitance of parallel plates scales with the inverse of their separation, so far more capacitive range is gained by decreasing the minimum displacement than by decreasing the maximum displacement, even when the trade is very unequal.

The flexure spring is readily stiffened by shorting or thickening the beams in each of the two stages, for stiffness scales cubically with both beam length and beam thickness. Increasing the stiffness of the structure also improves its moment rejection (Figure 4-13), a critical feature for the creation of planar fracture surfaces.

4.2.2 Constant Force Bias

A constant force bias could be added by placing a comb drive in parallel with the zipper and driving the comb drive at a fixed voltage. Doing so alters the equilibrium equation (Equation 4.10):

$$0 = -kx_0 - \frac{B}{x_0^2} + \frac{C}{\sqrt{\delta - x_0}} - F_p, \tag{4.22}$$

where F_p is the comb drive preload force (in milliNewtons, like the other forces), positive when acting to close the gap. This addition modifies the equilibrium polynomial

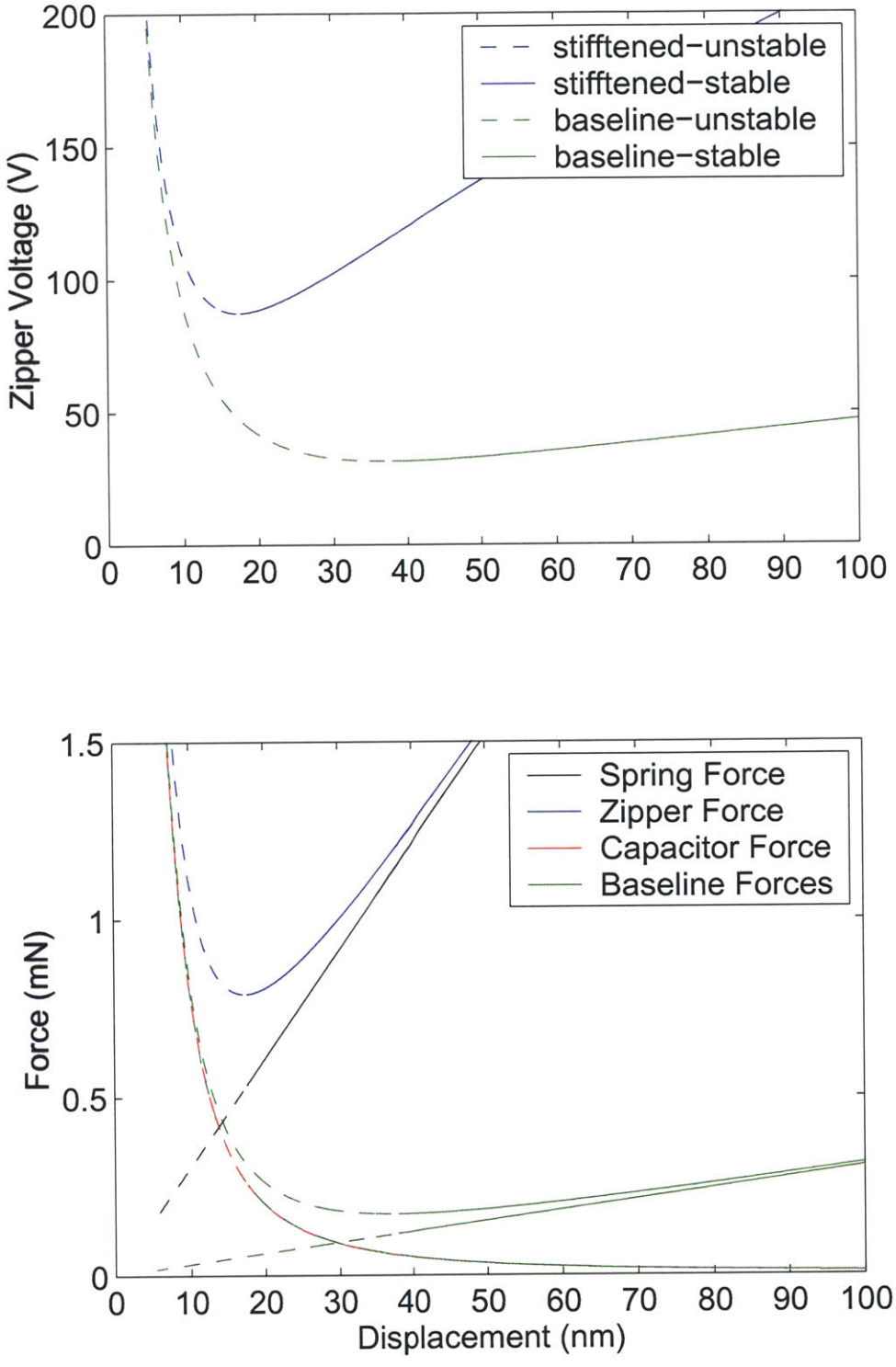


Figure 4-12: A reprise of Figure 4-11, but for the new stiffened flexure. The previous results are shown in green for comparison.

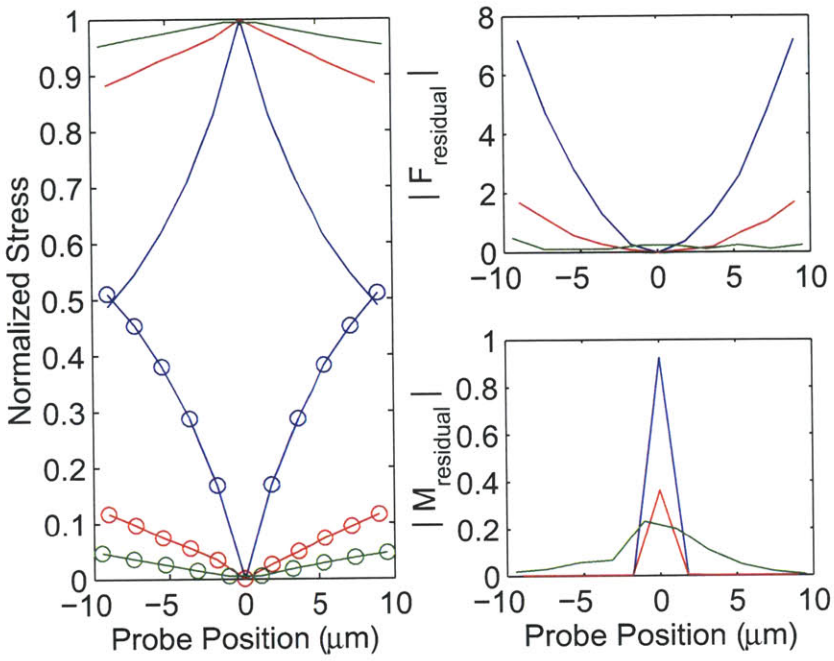


Figure 4-13: A plot of moment rejection for the single stage device (blue), the two stage device (red), and the stiffened variable capacitor device (green). Note that the circled line represents moment stress.

as follows (Equation 4.11):

$$\begin{aligned} 0 =& k^2 x_0^7 + (2F_p k - \delta k^2) x_0^6 + (F_p^2 - 2F_p \delta k^2) x_0^5 + (2BK + C^2 - F_p^2 \delta) x_0^4 \\ &+ (2F_p B - 2B\delta k) x_0^3 - 2F_p B \delta x_0^2 + B^2 x_0 - B^2 \delta. \end{aligned} \tag{4.23}$$

No modification of the equilibrium criterion (Equation 4.19) is necessary; F_p falls from the equation of motion when the solution is linearized about the equilibrium point. A analogous result is the invariance of a spring-mass system's natural frequency as the system's orientation is changed from horizontal to vertical.

Figure 4-14 shows how the force balance changes with the addition of a positive preload force. The new displacement curve is the blue line in the upper panel. The old displacement curve is the green line below it. The zipper voltage to achieve a particular displacement has been increased without decreasing the minimum stable

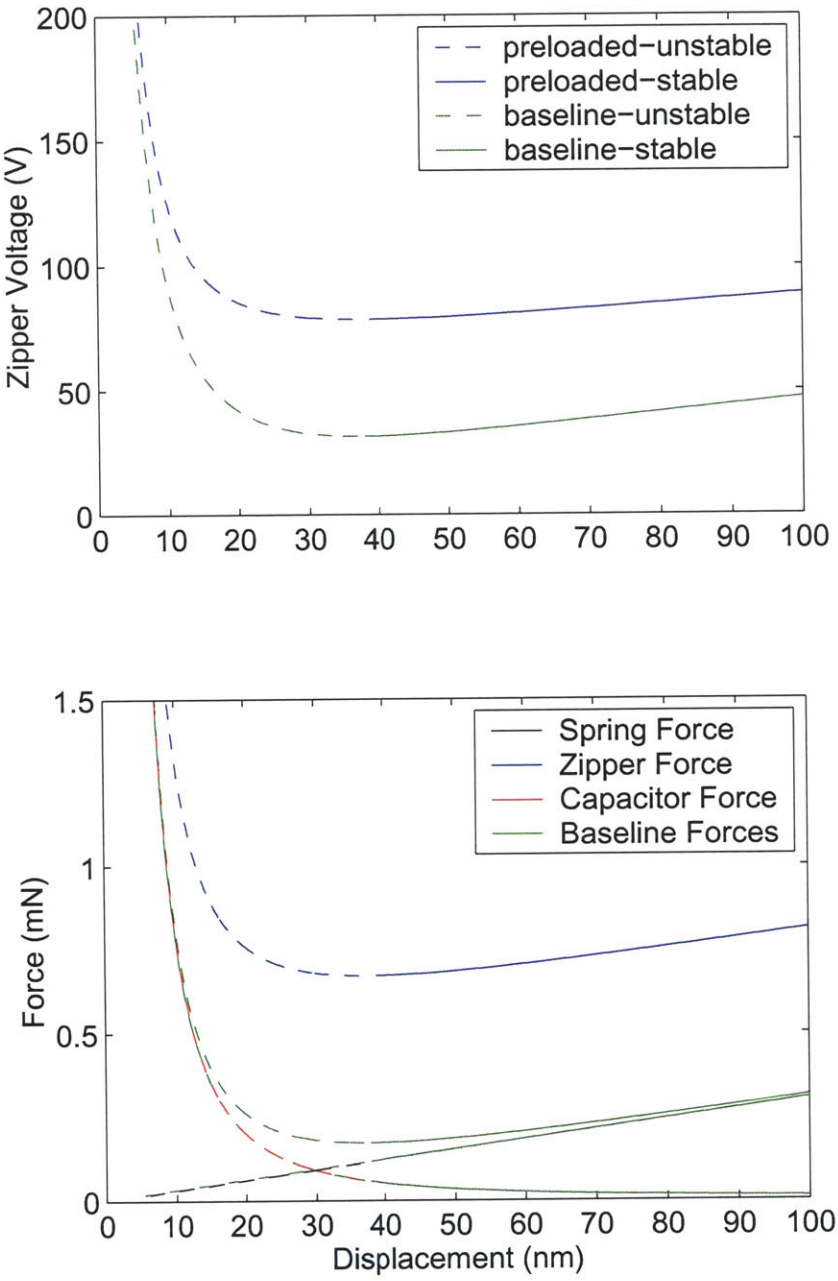


Figure 4-14: The equivalent of Figure 4-12 for a constant preload force. Note how the Zipper voltage (and zipper force) has increased for a given displacement, but that the minimum displacement has not.

gap opening. The preload force increases the force required from the zipper without improving small gap stability. This and the result from stiffening the flexure suggest that the truly important intersection is that between the flexure spring force and the capacitor force lines.

Changing the direction of the preload force does not improve performance either, as can be seen from Figure 4-15. For a gap opening preload, there are four valid solutions, two stable and two unstable. All have been plotted with respect to displacement in the top panel of the figure. The minimum stable solution (the left end of x_G) has not improved from the first analysis. Complexity has increased, however. Below approximately 18 V, there are now two stable equilibrium positions for the flexure, a controllability nightmare.

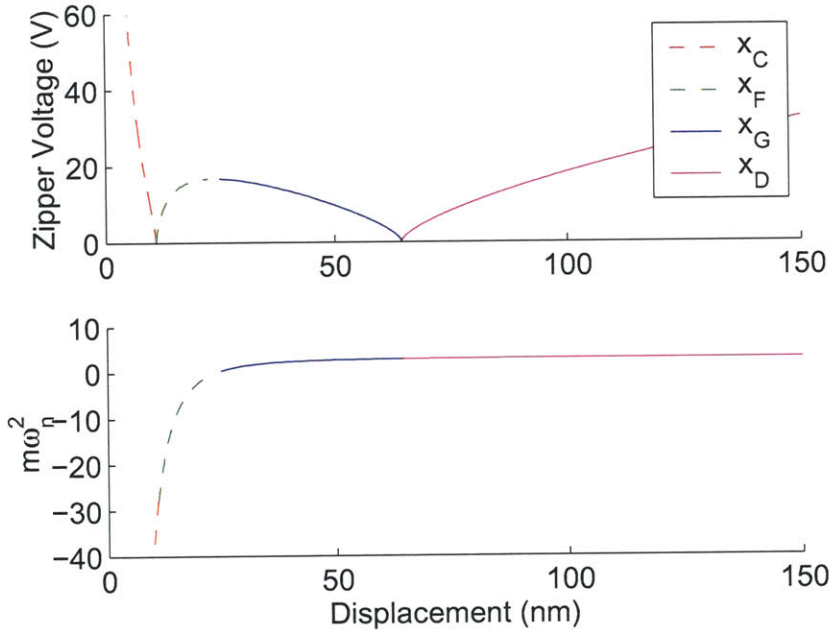


Figure 4-15: A plot of the four valid solutions for a positive (gap opening) preload. The dashed lines represent unstable solutions.

4.3 Three Node Model

After the single node model had been used to design the first prototype of the variable capacitor, some doubts arose about how accurately it represented the system. Two

node and three node models were constructed to resolve this uncertainty.

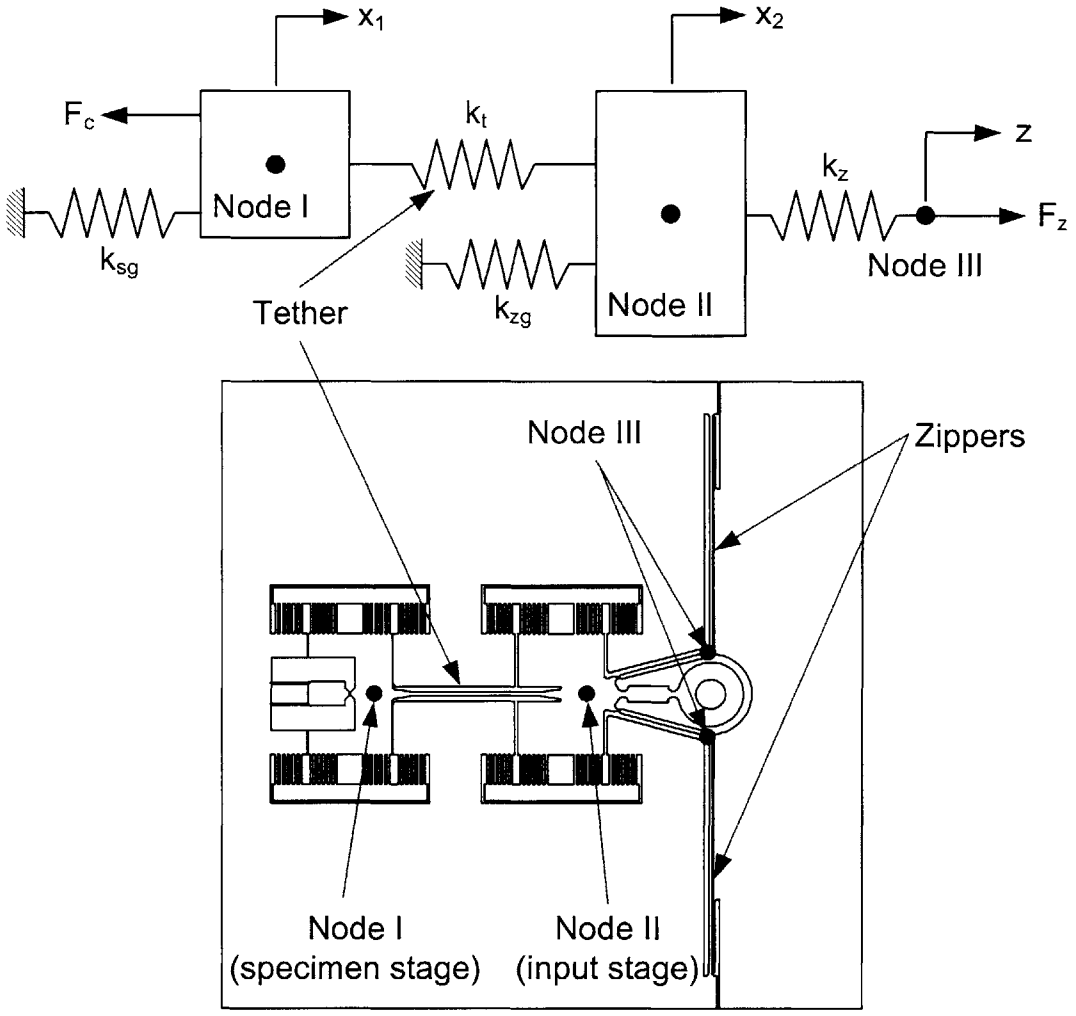


Figure 4-16: A three node model of the variable capacitor. Note the consolidation of the two zippers (and their connections to the flexure).

In Figure 4-16 the variable capacitor is modelled as a three node lumped parameter system. Node I is the specimen stage. Node II is the input stage of the flexure, and Node III is the zipper attachment point. This model deals only with displacements along the axis of the flexure; other motions are effectively damped by the structure. The two zippers (and their connections to the flexure) are consolidated into a single node because the zippers are always actuated together (and to simplify the analysis). The beams connecting the input stage (Node II) and the specimen stage (Node III)

to ground (the flexure frame) are represented by k_{zg} and k_{sg} respectively. The tether linking the two stages is represented by k_t.

4.3.1 Node I

As with the single node model, force equilibrium, $\Sigma F = 0$, is the starting point:

$$0 = F_{k_t} - F_{k_{sg}} - F_c, \tag{4.24}$$

and the forces are in turn replaced with their characteristic expressions:

$$0 = k_t(x_2 - x_1) - k_{sg}x_1 - \frac{B}{x_1^2}. \tag{4.25}$$

4.3.2 Node II

Repeating the procedure for Node II:

$$0 = -F_{k_t} - F_{k_{zg}} + F_{k_z} \tag{4.26}$$

$$0 = -k_t(x_2 - x_1) - k_{zg}x_2 + k_z(z - x_2) \tag{4.27}$$

4.3.3 Node III

Still a third time for Node III:

$$0 = -F_{k_z} + F_z \tag{4.28}$$

$$0 = -k_z(z - x_2) + \frac{C}{\sqrt{\delta - z}} \tag{4.29}$$

4.3.4 Mathematical Difficulties

Unfortunately, these equations become intractable. Equation 4.25 for Node I can be solved for x_2:

$$x_2 = x_1\left(1 + \frac{k_{sg}}{k_t}\right) + \frac{B}{k_t x_1^2}, \tag{4.30}$$

and substituted into the Node II Equation 4.27:

$$\begin{aligned} 0 = \;& k_z\left(z - x_1\left(1 + \tfrac{k_{sg}}{k_t}\right) - \tfrac{B}{k_t x_1^2}\right) \\ - \;& k_{zg}\left(x_1\left(1 + \tfrac{k_{sg}}{k_t}\right) + \tfrac{B}{k_t x_1^2}\right) \\ + \;& k_t\left(x_1\left(1 + \tfrac{k_{sg}}{k_t}\right) + \tfrac{B}{k_t x_1^2} - x_1\right) \end{aligned} \tag{4.31}$$

leaving an equation where x_1 and z are the only unknowns, but solving Equation 4.29 for z in terms of x_2, which is merely a step along the path towards solving it for x_1, results in a cubic equation:

$$z^3 - (2x_2 + \delta)\, z^2 + \left(x_2^2 + 2\delta x_2\right) z + \left(\frac{C^2}{K_2^2} - \delta x_2^2\right) = 0, \tag{4.32}$$

that is difficult to substitute into Equation 4.31.

The problem could be overcome by carrying through all three of the cubic formula solutions, but that would treble the complexity of a model that was primarily intended to confirm the predictions of a simpler previous model. A more attractive solution presented itself upon evaluation of the various spring constants, see Figure 4-17. The relative stiffness of the zippers' connection with the input stage suggested consolidation of those two nodes, removing the cubic equation.

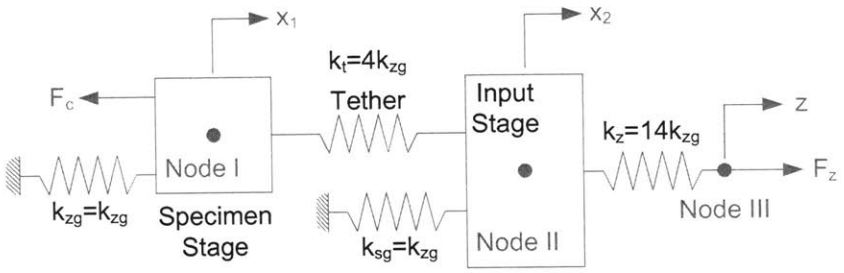


Figure 4-17: The relative values of the various spring constants in the three node model. Note the relative stiffness of the zipper input spring (k_z)

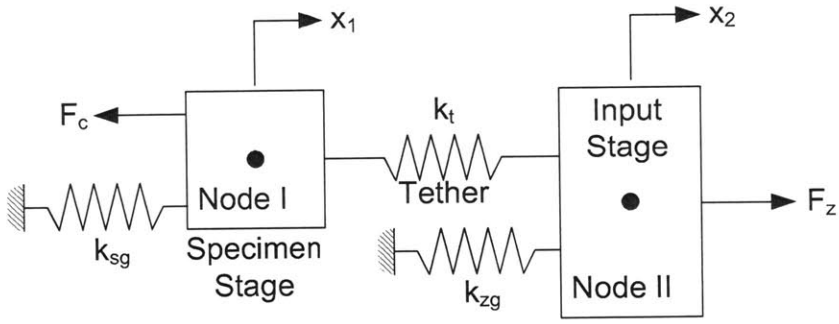


Figure 4-18: A revision of the three node model with Nodes II and III consolidated by the elimnation of spring k_z.

4.4 Two Node Model

The consolidation of Nodes II and III with the elimination of the spring associated with the zipper to flexure connection (k_z) results in a model like that seen in Figure 4-18.

Consolidation leaves the Node I equations unchanged and alters the Node II equations as follows:

$$0 = F_z - F_{k_t} - F_{k_{zg}} \tag{4.33}$$

$$0 = \frac{C}{\sqrt{\delta - x_2}} - k_t(x_2 - x_1) - k_{zg}(x_2) \tag{4.34}$$

Substituting Equation 4.30 into Equation 4.34 yields an expression with x_1 as the only unknown:

$$
\begin{aligned}
0 = & \frac{C}{\sqrt{\delta - (1 + \frac{k_{sg}}{k_t})x_1 - \frac{B}{k_t x_1^2}}} \\
& -k_t \left(\frac{k_{sg}}{k_t} x_1 + \frac{B}{k_t x_1^2} \right) \\
& -k_{zg} \left(\left(1 + \frac{k_{sg}}{k_t} \right) x_1 + \frac{B}{k_t x_1^2} \right)
\end{aligned} \tag{4.35}
$$

Consolidating terms:

$$
0 = \frac{C}{\sqrt{\delta - \left(1 + \frac{k_{sg}}{k_t}\right) x_1 - \frac{B}{k_t x_1^2}}} - \left(k_{sg} + k_{zg} + \frac{k_{sg} k_{zg}}{k_t} \right) x_1 - \left(1 + \frac{k_{zg}}{k_t} \right) \frac{B}{x_1^2} \tag{4.36}
$$

At this point, the constant terms can be simplified:

$$
0 = \frac{C}{\sqrt{\delta - \psi x_1 - \frac{\eta}{x_1^2}}} - \phi x_1 - \frac{\theta}{x_1^2} \tag{4.37}
$$

where

$$
\phi = k_{sg} + k_{zg} + \frac{k_{sg} k_{zg}}{k_t} \tag{4.38}
$$

$$
\theta = \left(1 + \frac{k_{zg}}{k_t} \right) B \tag{4.39}
$$

$$
\psi = 1 + \frac{k_{sg}}{k_t} \tag{4.40}
$$

$$
\eta = \frac{B}{k_t} \tag{4.41}
$$

.

Manipulating the equation into a polynomial yields:

$$0 = \begin{bmatrix} x_1^9 & x_1^8 & x_1^7 & x_1^6 & x_1^5 & x_1^4 & x_1^3 & x_1^2 & x_1 & 1 \end{bmatrix} \cdot \begin{bmatrix} -\psi\phi^2 \\ \delta\phi^2 \\ 0 \\ -(2\phi\theta\psi + \phi^2\eta + C^2) \\ 2\phi\theta\delta \\ 0 \\ -(\theta^2\psi + 2\theta\phi\eta) \\ \delta\theta^2 \\ 0 \\ -\theta^2\eta \end{bmatrix} \tag{4.42}$$

Solving the polynomial yields solutions ($x_1 = x_0$) to the equilibrium equation (Equation 4.37); for $x_1 = x_0$, the forces sum to zero.

4.4.1 Model Implementation

Matlab code for implementing the two-node model described in the previous section is contained in Appendix D.1. Being of greater than fourth order, the polynomial (Equation 4.42) is solved numerically. The non-physical solutions are then stripped out and the viable solutions automatically stitched together. Linking the solutions together automatically enabled the system optimization that will be discussed in Section 4.5.

4.4.2 Stability Analysis

The strategy for determining the stability of the equilibrium points in the two-node model is the multi degree-of-freedom analog of the strategy employed for the single-node model. The squared linearized natural frequencies, $\tilde{\omega}_n^2$, of each node are the eigenvalues of the matrix $\mathsf{M}^{-1}\mathsf{K}$, where the matrices M and K are defined by the equation

$$0 = \mathsf{M} \begin{bmatrix} \ddot{x}_{1p} \\ \ddot{x}_{2p} \end{bmatrix} + \mathsf{K} \begin{bmatrix} x_{1p} \\ x_{2p} \end{bmatrix}, \tag{4.43}$$

where, x_{1p} and x_{2p} are perturbations from the Node I and Node II equilibrium positions. If the squares of both linearized natural frequencies are positive, the equilibrium is stable. If either is negative, the system is unstable.

Node I

Based on Equation 4.25, the equation of motion for Node I is

$$m_1 \ddot{x}_1 = k_t \left(x_2 - x_1\right) - k_{sg} x_1 - \frac{B}{x_1^2}, \tag{4.44}$$

where m_1 is the mass at that node. Rewriting the equilibrium with x_{10} and x_{20} as the equilibrium positions, Equation 4.25 becomes:

$$0 = k_t(x_{20} - x_{10}) - k_{sg} x_{10} - \frac{B}{x_{10}^2}. \tag{4.45}$$

For small perturbations, x_{1p} and x_{2p}, about the equilibrium positions, x_{10} and x_{20}, Equation 4.44 is rewritten as:

$$0 = m_1(\ddot{x}_{10} + \ddot{x}_{1p}) - k_t \left(x_{20} + x_{2p} - x_{10} - x_{1p}\right) + k_{sg} \left(x_{10} + x_{1p}\right) + \frac{B}{\left(x_{10} + x_{1p}\right)^2} \tag{4.46}$$

Realizing that $\ddot{x}_{10} = 0$ and substituting for the non-linear term yields:

$$0 = m_1 \ddot{x}_{1p} - k_t \left(x_{20} + x_{2p} - x_{10} - x_{1p}\right) + k_{sg} \left(x_{10} + x_{1p}\right) + T_1 \left(x_{10} + x_{1p}\right), \tag{4.47}$$

where

$$\begin{aligned} T_1(x_{10}+x_{1p}) &= \frac{B}{(x_{10}+x_{1p})^2} \\ &\approx T_1(x_{1p}=0) + x_{1p}\left.\frac{\mathrm{d}T_1}{\mathrm{d}x_{1p}}\right|_{x_{1p}=0} \\ &\approx \frac{B}{x_{10}^2} - \frac{2B}{x_{10}^3}x_{1p}. \end{aligned} \tag{4.48}$$

Substituting the linearized term back into Equation 4.47 yields

$$0 = m\ddot{x}_{1p} - k_t(x_{20}+x_{2p}-x_{10}-x_{1p}) + k_{sg}(x_{10}+x_{1p}) + \frac{B}{x_{10}^2} - \frac{2B}{x_{10}^3}x_{1p}. \tag{4.49}$$

Subtracting the equilibrium equation (Equation 4.45) reduces the expression to

$$0 = m\ddot{x}_{1p} - k_t(x_{2p}-x_{1p}) + k_{sg}x_{1p} - \frac{2B}{x_{10}^3}x_{1p}, \tag{4.50}$$

which can in turn be consolidated into

$$0 = m\ddot{x}_{1p} + x_{1p}\left(k_{sg}+k_t-\frac{2B}{x_{10}^3}\right) + x_{2p}(-k_t). \tag{4.51}$$

Node II

Turning to Node II, the equation of motion (based on Equation 4.34) is

$$m_2\ddot{x}_2 = \frac{C}{\sqrt{\delta - x_2}} - k_t(x_2-x_1) - k_{zg}x_2, \tag{4.52}$$

where m_2 is the mass at the node. Rewriting the equilibrium equation with x_{10} and x_{20} as the equilibrium positions, Equation 4.34 becomes

$$0 = \frac{C}{\sqrt{\delta - x_{20}}} - k_t(x_{20}-x_{10}) - k_{zg}x_{20}. \tag{4.53}$$

For small perturbations, x_{1p} and x_{2p}, about the equilibrium positions, x_{10} and x_{20},

Equation 4.52 becomes:

$$m_2(\ddot{x}_{20} + \ddot{x}_{2p}) = \frac{C}{\sqrt{\delta - x_{20} - x_{2p}}} - k_t\left(x_{20} + x_{2p} - x_{10} - x_{1p}\right) - k_{zg}\left(x_{20} + x_{2p}\right). \quad (4.54)$$

After inputting $\ddot{x}_{20} = 0$ and substituting for the non-linear term, the equation of motion becomes

$$0 = m_2\ddot{x}_{2p} - T_2\left(x_{20} + x_{2p}\right) + k_t\left(x_{20} + x_{2p} - x_{10} - x_{1p}\right) + k_{zg}\left(x_{20} + x_{2p}\right), \quad (4.55)$$

where

$$\begin{aligned} T_2\left(x_{20} + x_{2p}\right) &= \frac{C}{\sqrt{\delta - x_{20} - x_{2p}}} \\ &\approx T_2\left(x_{2p} = 0\right) + x_{2p}\left.\frac{\mathrm{d}T_2}{\mathrm{d}x_{2p}}\right|_{x_{2p}=0} \\ &\approx \frac{C}{\sqrt{\delta - x_{20}}} + \frac{C}{2\left(\delta - x_{20}\right)^{\frac{3}{2}}} x_{2p}. \end{aligned} \quad (4.56)$$

Substituting the linearized term back into Equation 4.55 yields

$$\begin{aligned} 0 &= m_2\ddot{x}_{2p} - \frac{C}{\sqrt{\delta - x_{20}}} - \frac{C}{2\left(\delta - x_{20}\right)^{\frac{3}{2}}} x_{2p} \\ &\quad + k_t\left(x_{20} + x_{2p} - x_{10} - x_{1p}\right) + k_{zg}\left(x_{20} + x_{2p}\right). \end{aligned} \quad (4.57)$$

Subtracting the equilibrium equation (Equation 4.53) reduces the expression to

$$0 = m_2\ddot{x}_{2p} - \frac{C}{2\left(\delta - x_{20}\right)^{\frac{3}{2}}} x_{2p} + k_t\left(x_{2p} - x_{1p}\right) + k_{zg}\left(x_{2p}\right). \quad (4.58)$$

which can in turn be consolidated into

$$0 = m_2\ddot{x}_{2p} + x_{1p}\left(-k_t\right) + x_{2p}\left(k_t + k_{zg} - \frac{C}{2\left(\delta - x_{20}\right)^{\frac{3}{2}}}\right). \tag{4.59}$$

Matrix Representation

Combining the linearized equation of motion for Node I (Equation 4.51) and the linearized equation of motion for Node II (Equation 4.59) yields the equation

$$0 = \begin{bmatrix} m_1 & 0 \\ 0 & m_2 \end{bmatrix}\begin{bmatrix} \ddot{x}_{1p} \\ \ddot{x}_{2p} \end{bmatrix} + \begin{bmatrix} k_{sg} + k_t - \frac{2B}{x_{10}^3} & -k_t \\ -k_t & k_t + k_{zg} - \frac{C}{2(\delta - x_{20})^{\frac{3}{2}}} \end{bmatrix}\begin{bmatrix} x_{1p} \\ x_{2p} \end{bmatrix}. \tag{4.60}$$

Based on this definition of the mass matrix, M, and the stiffness matrix, K, the eigenvalues of $\mathsf{M}^{-1}\mathsf{K}$ are calculated at each equilibrium point. As with the analysis of the single-node model, the result is that the equilibrium dominated by the zipper force and the capacitive force (the diamonds in Figure 4-4) is unstable, while the equilibrium dominated by the zipper force and the spring force (the circles in Figure 4-4) is stable. The result was not affected by reasonable changes in the ratio of the masses, m_1 and m_2, at each node.

4.5 Optimization Studies

The two-node model was used for a series of optimization studies. The parameters varied included, the zipper beam height (h), the zipper stroke (Δ), the specimen stage stiffness (k_{sg}), the input stage stiffness (k_{zg}), and the tether stiffness (k_t). The device performance characteristics studied were the maximum displacement (x_{max}), the minimum displacement (x_{min}), and the minimum actuator voltage (V_{min}).

Of the three output parameters, minimum displacement is the most important. Obtaining the smallest stable separation of the two fracture surfaces has been a major goal from the very beginning. To the extent it could be effected without enlarging the minimum separation, another goal of the optimization was to increase the maximum displacement. A larger maximum displacement improves performance slightly,

and makes it more likely the displacement of the surfaces can be directly observed. Decreasing the voltage at which the minimum displacement occurs, V_{min}, is advantageous because in the event of crosstalk between the actuator and the capacitance measurement circuit, the actuator voltage that must be rejected by the measurement circuit is reduced.

On each of the plots in the following sub-sections, circles indicate the performance of the final design (Table 4.1). When studying the effect of a particular parameter, the values of the other parameters were set to those of the final design. Naturally, this was an iterative process, of which only the final step is shown here.

4.5.1 Zipper Beam Height (h)

Figure 4-19 plots the results of the design optimization for varying the zipper beam height. Minimum surface separation is independent of zipper beam height (the $\pm 0.1\,\text{nm}$ variations are numerical noise), and both the minimum voltage and the maximum displacement trends argue for increasing the beam height. Beam height was therefore increased to $30\,\mu\text{m}$ from $20\,\mu\text{m}$ in the first prototype. Reluctance to move very far from the baseline device precluded a larger change.

4.5.2 Zipper Stroke (Δ)

Figure 4-20 plots the results of the design optimization for varying the zipper stroke. As was the case with beam height, minimum surface separation is independent of zipper stroke (the $\pm 0.1\,\text{nm}$ variations are numerical noise). Both the minimum voltage and the maximum displacement trends favor the smallest feasible Δ; the minimum value compatible with our mask making lithographic processes, $3\,\mu\text{m}$, was adopted.

4.5.3 Flexure Stage Stiffnesses (k_{sg} and k_{zg})

Figure 4-21 plots the results of the design optimization for varying the specimen stage stiffness and the input stage stiffness. The trends for the minimum voltage and maximum displacement argue for more compliance, while the minimum displacement

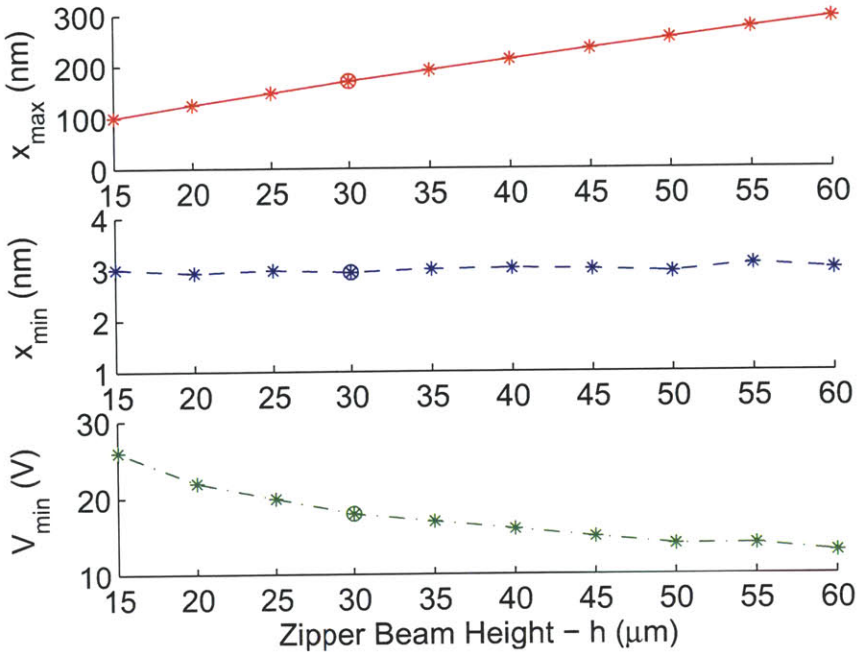


Figure 4-19: Device performance parameters as a function of zipper beam height, h. The circles mark the performance of the final design. A larger value for the zipper beam height was not used out of concern for choosing a value too far from the established performance envelope of the actuator. The 0.1 nm fluctuations in the x_{min} plot are numerical noise.

trend favors an increase in the stiffness. Because the trends break in opposing directions, a compromise value of approximately 17 $\frac{\text{mN}}{\mu\text{m}}$ was selected for both spring constants. The compromise value is at the "knee" of both curves and results in good performance for all three parameters.

4.5.4 Tether Stiffness (k_t)

Figure 4-22 plots the results of the design optimization for varying the tether stiffness. The stiffness of the tether connecting the two flexure stages has very little impact on the performance of the device. Doubtless, the outcome would have been different if the tether were not already the stiffest spring in the network. Because of its lack of influence on the device's performance as a capacitor and its criticality to the proper fracture fabrication of the surfaces, the stiffness of the tether was not changed from that of the baseline device.

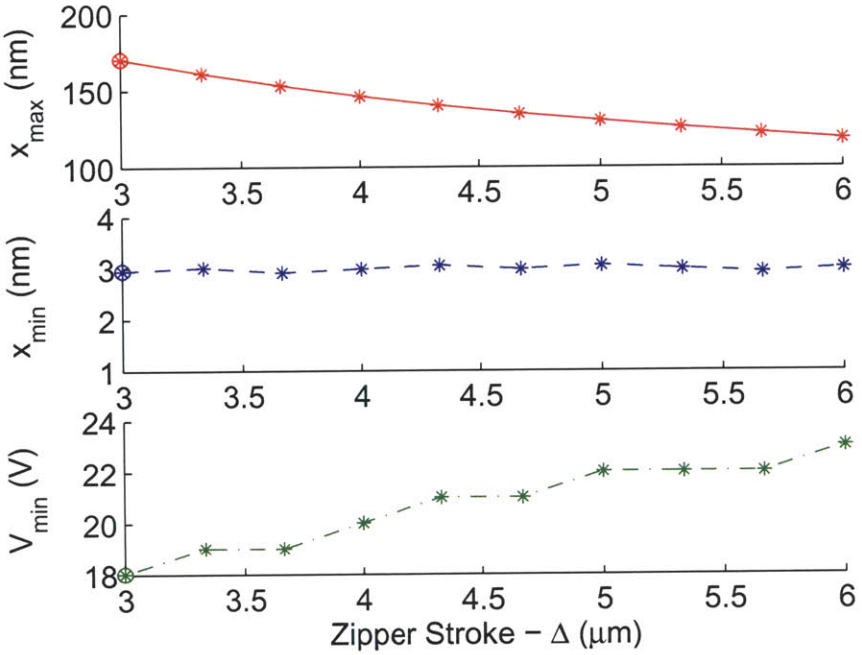
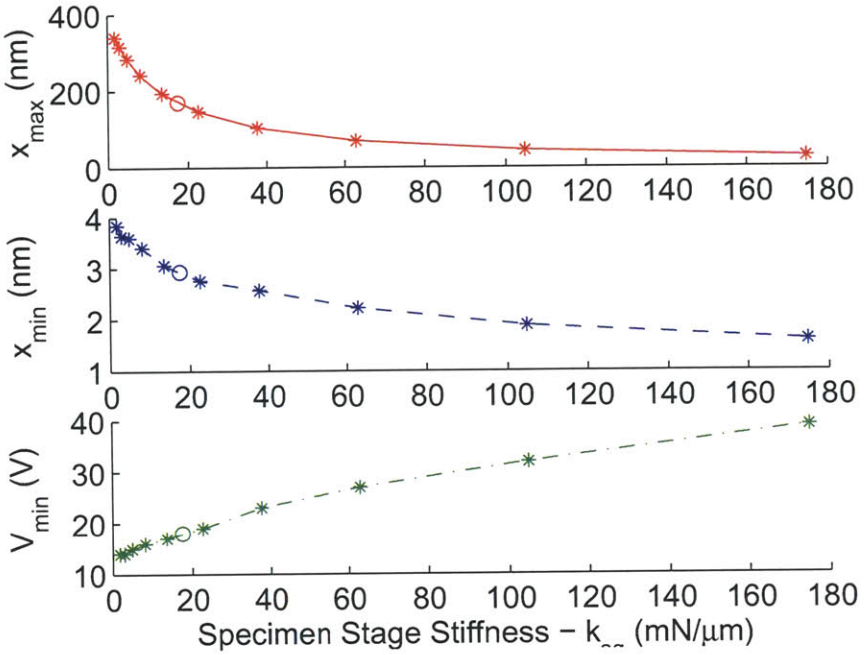


Figure 4-20: Device performance parameters as a function of zipper stroke, Δ. The circles mark the performance of the final design.

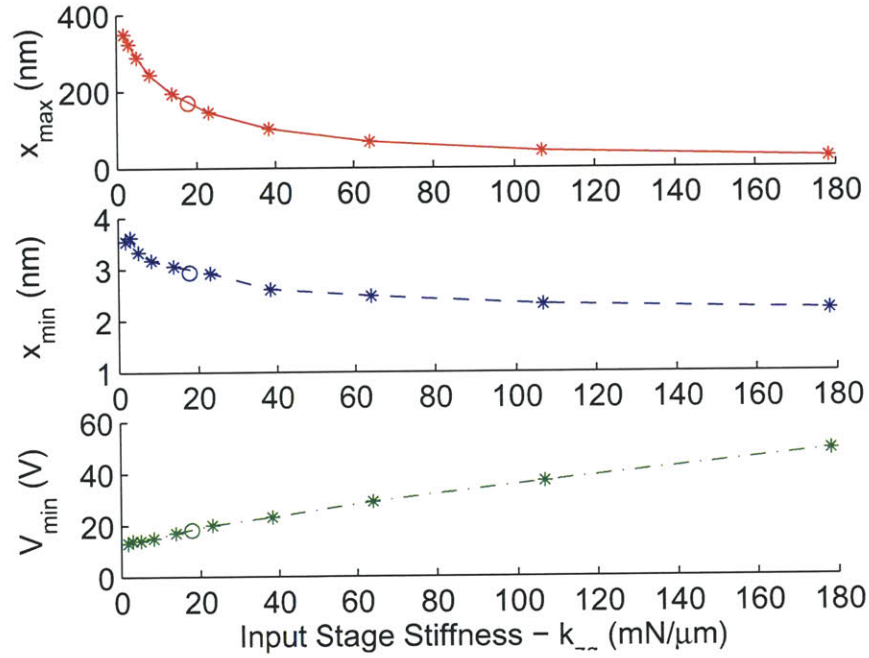
4.5.5 Optimized Parameter Values

The values for the optimized design parameters are in Table 4.1. As with the previous model, the primary driver of performance is the comparative forces of the capacitor and the compliant structure; the system is stable with the actuator working against one but not the other. Reduction mechanisms, stronger actuators, and independent parallel actuators can improve the device at the periphery (lower voltage operation, larger maximum stroke, etc.), but they do not alter this central relationship. Reducing the capacitor's excitation does improve performance, so it was done to the extent compatible with making a good measurement.

For equivalent model parameters, the difference between the single node and two node models was negligible, confirming the validity of the single node model used to develop the first prototype. The two node model did, however, facilitate the independent optimization of design parameters not available with just a single node. The plot in Figure 4-23 describes the performance of the optimized device.



(a) Device performance parameters as a function of specimen stage stiffness, k_{sg}.



(b) Device performance parameters as a function of zipper stage stiffness, k_{zg}

Figure 4-21: Design study results for the flexure stage stiffnesses. The circles mark the performance of the final design.

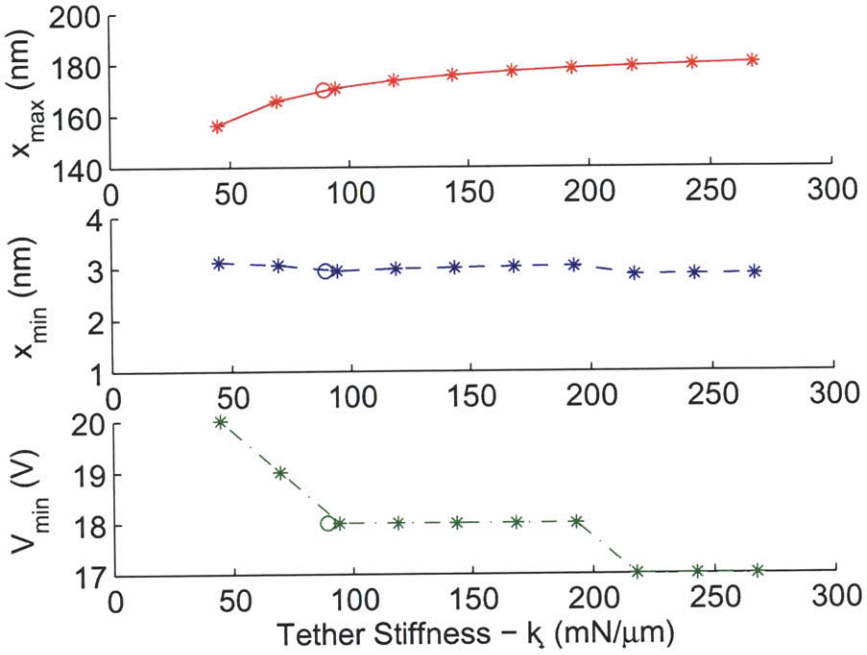


Figure 4-22: Device performance as a function of tether stiffness, k_t. The circles mark the performance of the final design.

4.6 Dielectric Breakdown

Breakdown is a concern both when the fracture surfaces are in contact and when they are separated. Ideally, breakdown does not occur in either case, and the pull-in instability limits performance. Then, when pull-in does occur, it will not damage the device. If breakdown occurs across the silicon oxide on the in-contact fracture surfaces, a pull-in event may destroy the device, so the instability should be assiduously avoided. If breakdown takes place across an open gap larger than the pull-in gap, pull-in is no longer performance limiting, and our optimization of the actuator-flexure system was for naught.

4.6.1 Silicon Oxide (Zero Separation) Breakdown

No experiments on the breakdown of native oxide were found in the literature, so the breakdown voltage was estimated using a reasonable value of silicon oxide's dielectric strength and the anticipated thickness of the native oxide on the fracture faces.

Zipper Beam Height	h	$30\,\mu\text{m}$
Zipper Stroke	Δ	$3\,\mu\text{m}$
Input Stage Stiffness	k_{sg}	$17.8\left(\frac{\text{mN}}{\mu\text{m}}\right)$
Specimen Stage Stiffness	k_{zg}	$17.5\left(\frac{\text{mN}}{\mu\text{m}}\right)$
Tether Stiffness	k_t	$89.2\left(\frac{\text{mN}}{\mu\text{m}}\right)$

Table 4.1: Summary of the values for the parameters chosen as a result of the design study.

Within the literature, there is considerable variation in native oxide thickness measurements, but it is likely between 1.4 to 2.5 nm ([117, 89, 25]) thick. Fortunately, oxide forms more quickly on fractured surfaces than on the etched surfaces on which it is typically grown. Highly doped silicon (like that from which the devices will be fabricated) is a fast oxidizing substrate, and about 1.1 – 1.3 nm of oxide should grow on both faces within several hours of exposure [117]. The coating should also be reasonably uniform; native oxide has been used as an etch mask [50].

Values for the dielectric strength of silicon oxide range from $2 \cdot 10^6$ to $5 \cdot 10^6 \frac{\text{V}}{\text{cm}}$ [89, 8], but those measurements were not made on native oxide. Using the lower end of the range, $2 \cdot 10^6 \frac{\text{V}}{\text{cm}}$, as the dielectric strength of the oxide (and remembering that oxide is on both faces), gives a breakdown voltage of 0.4 to 1.0 V, depending on the value of the oxide thickness chosen.

Operating at a low voltage to prevent breakdown dovetails nicely doing the same to support the minimization of the stable surface separation.

4.6.2 Gas Dielectric (Positive Separation) Breakdown

Extrapolation from Wong's data [148] indicates breakdown of the air between the faces of the capacitor will not be a problem. Wong's data is plotted in Figure 4-24 along with the relevant pressure-distance products for the capacitor (assuming a larger than planned potential of 25 V). His data is divided into two sets. The "good"

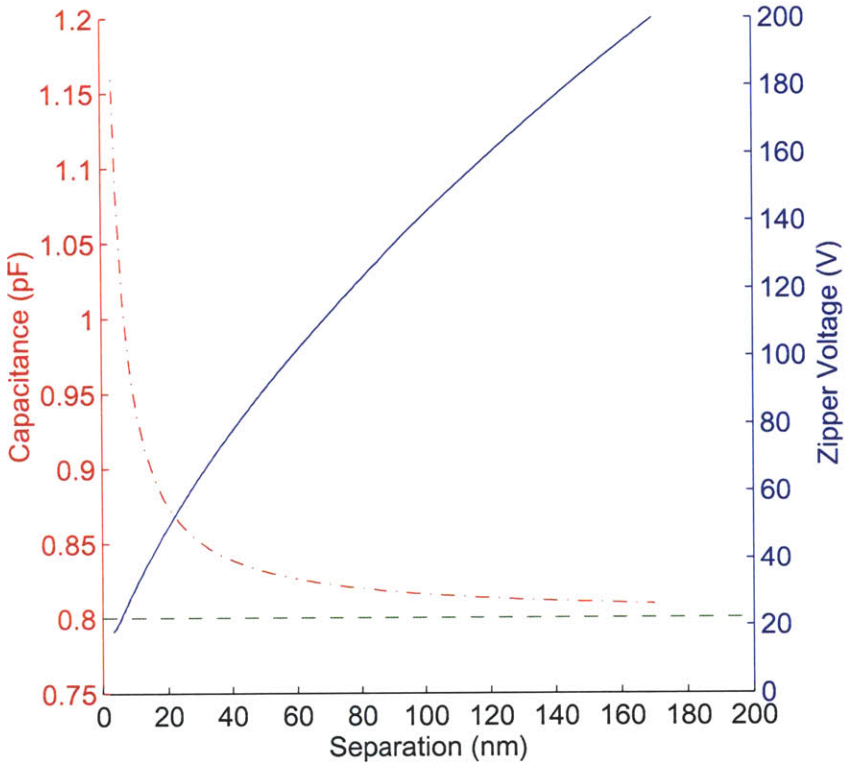


Figure 4-23: Final performance of the optimized device. The dashed horizontal line represents the parasitic capacitance.

data from devices with breakdown voltages greater than or equal to 270 V and the "suspect" data from devices with breakdown voltages less than or equal to 176 V. He attributed this split to die-saw debris contamination of the suspect devices. Changing the post die-saw cleaning procedure altered the proportion of good to suspect devices from one in two to one in ten.

Despite setting a larger than planned potential of 25 V across the plates, the variable capacitor's line is always considerably below Wong's good data. It is also below the 360 V minimum in the pressure-distance curve [19] generally used as a conservative estimate. This margin may be necessary, however, for any crenellations on the surface will concentrate the field and precipitate breakdown at a voltage lower than would be expected from a uniform field.

Wong's data is unusual in that he achieved the low pressure-distance products at small distances and atmospheric pressure rather than with large distances but low

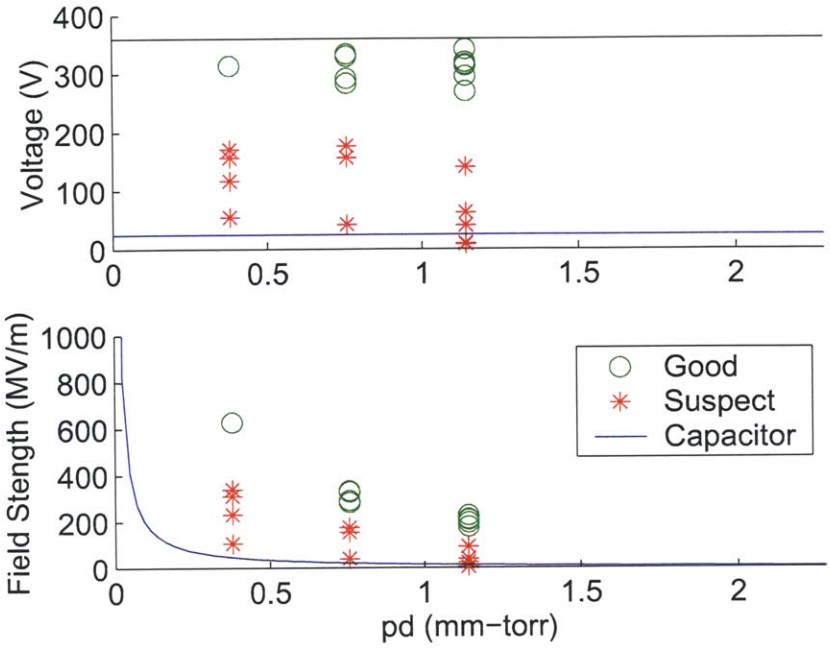


Figure 4-24: A plot of breakdown field strength data from Wong [148] along with the field strength or operating voltage between the plates of the capacitor at different gap openings.

pressures. Nevertheless, there is some risk in extrapolation. His minimum gap was 500 nm, roughly one hundred times greater than the gaps at which the current device will operate.

Still another concern is field emission of electrons. Assuming this will occur at field strengths greater than $10^9 \frac{\mathrm{V}}{\mathrm{m}}$, the gap at which it becomes an issue is the same as the voltage applied across the faces, expressed in nanometers, so for our anticipated operating point of 1 V, field emission should not be a problem until the surfaces are within 1 nm of each other.

4.7 The First Prototype

The first prototype design (Figure 4-25) consists primarily of a stiffened two stage device onto which a zipper actuator has been added. The zipper was connected to the input stage rather than the specimen stage to minimize the changes necessary to the device geometry and so the full moment attenuating capability of the structure

would be available should the output of the zipper be non-ideal. Among the other features incorporated were adhesive flow control, "epoxy," holes, breakout tabs, and electrical contacts.

4.7.1 Handle Layer Relief

To facilitate release of the device layer structure, i.e. the zipper and the flexure, the handle layer beneath it is etched to create a relief. Although this is a design detail, it's principal impact is on fabrication, so it will be covered more thoroughly in Chapter 5.

4.7.2 Die Attach Flow Control Holes

Holes were etched in the handle layer in an L-shaped pattern around the device layer structure. These holes prevent adhesive from flowing up into the handle layer relief during assembly.

4.7.3 Breakout Tabs

The device layer structure was considered too fragile for the die-saw, so the handle layer around each die was removed except for four tabs that were subsequently fractured with a probe to fully separate the die. The chief downside of this operation was the production of many small particles that could have (but did not) interfere with operation of the device. See Section 5.1.6 for further discussion on this topic.

4.7.4 Electrical Contacts

Specific areas of the device were set aside for electrical contacts. These areas were not exposed during the thermal oxidation required to fabricate the zipper actuator, leaving the bare silicon there available for wire bonding. See Appendix B.1 for a diagram mapping the electrical contact pads to package pins.

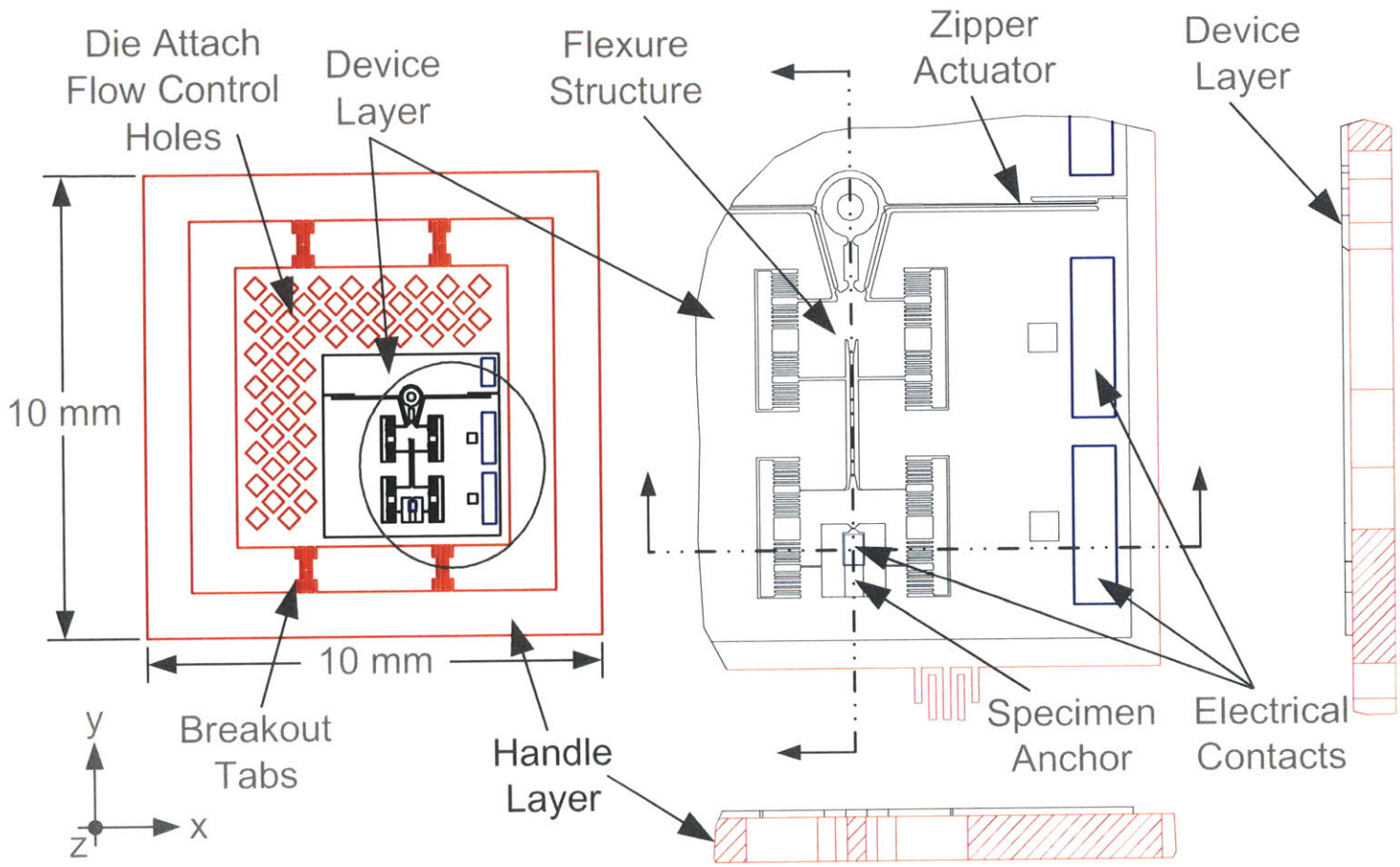
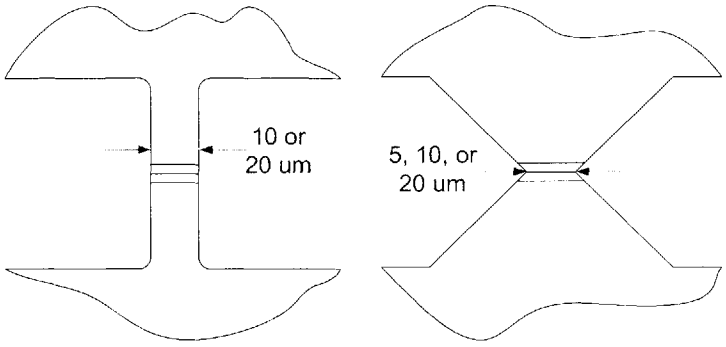


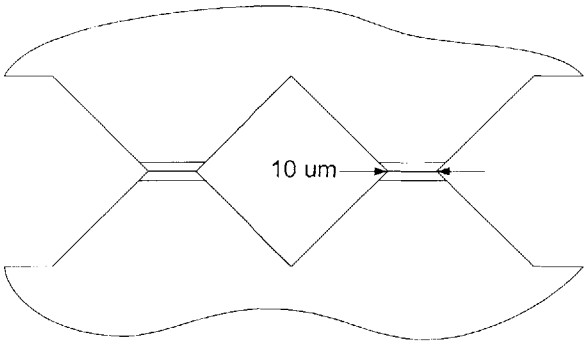
Figure 4-25: The variable capacitor design

4.7.5 Fracture Specimen Types

Six different specimen types were fabricated into otherwise almost identical dies. The different types were: 5 μm, 10 μm, and 20 μm wide hourglasses, 10 μm and 20 μm wide straight specimens, and 10 μm wide double hourglass specimens (Figure 4-26). The different specimen widths were introduced to study the effect of that variation on the fracture surfaces. Straight specimens were included to determine whether they would serve as well as the hourglass specimens. In the course of developing the fracture process, it was observed that the KOH notch was often imperfectly aligned with the waist of the hourglass. This misalignment seemed to do no harm, which suggested the hourglass shape served no purpose, and was thus ripe for removal. The double specimen was included to see if simultaneous fracture at multiple points could be effected and produce high quality surfaces. Hourglass shaped specimens were used because they were the baseline shape.



(a) Straight Specimens (b) Hourglass Specimens

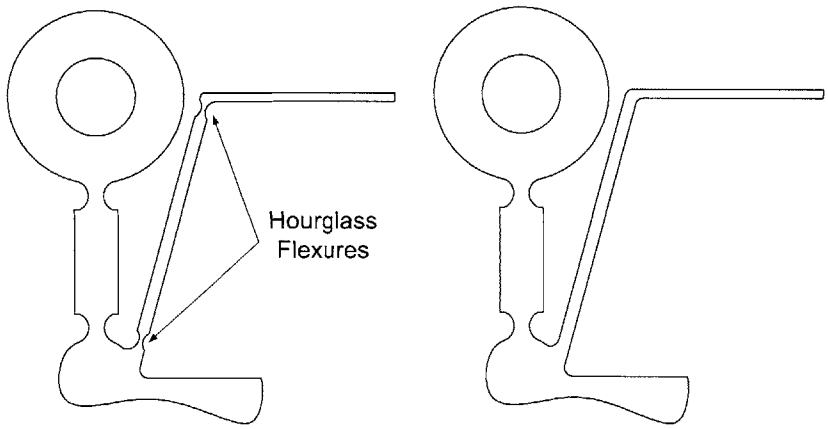


(c) Double Hourglass Specimen

Figure 4-26: First prototype specimen types.

4.7.6 Zipper Connection

Two different types of zipper connections were also included (Figure 4-27). The direct connection attaches the zipper to the body of the input stage with a straight link. The other (more common) type employed a pair of hourglass flexures at either end of the link. FEA indicated the flexures reduce the moment stiffness of their links to 44% of the stiffness of the straight links, thereby improving the fidelity of the zipper model, which did not include moment effects. Direct connections were only included at all out of an excess of caution about the potential for failure of the structure at the hourglasses; in the event, none failed.



(a) Hourglass flexure connection (b) Direct connection

Figure 4-27: The two types of zipper connection

4.8 Summary

A variable capacitor employing fracture fabricated surfaces has been designed. Design parameters such as the flexure stiffnesses, the actuator dimensions, and the capacitor excitation potential were varied to minimize the achievable stable separation between the two fracture surfaces. The physical insight associated with minimizing the stable separation of the surfaces is that the system is stable when the zipper is working against the structure's stiffness, but not when it's working against the electrostatic force pulling the two fracture surfaces together. Based on that insight, the structure

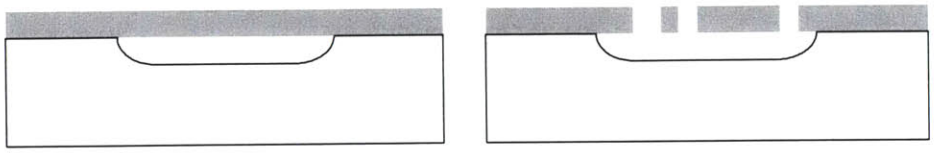
was stiffened and the potential across the capacitor surfaces reduced so the spring force dominates at a reduced surface separation. The increased stiffness of the complaint mechanism reduces the maximum stroke of the device, but this does not substantially affect the tuning ratio because the capacitance so rapidly begins to asymptotically approach the value of the parasitics as surface separation increses. Features were also added to the design to facilitate electrical contact, die singulation, and assembly. Fabrication and testing of the device are discussed in Chapter 5.

Chapter 5

Variable Capacitor Fabrication and Testing

The variable capacitor fabrication process is based on a SOI accelerometer process from Amini [1] (other similar processes include [131] and [97]). For that process, the handle layer is DRIE'd down to the buried oxide, creating a relief, the buried oxide is etched, and then the accelerometer structure is etched into the device layer. Because the handle layer has been relieved, there is no surface against which the device layer structure can become stuck. With the addition of a KOH etch to notch the specimens, some nitride patterning to create electrical contact pads, and a thermal oxidation, the accelerometer process becomes the variable capacitor process.

An alternative process similar to [58] and [126] employing a bonded silicon-glass wafer (Figure 5-1) was also considered, but too much process development would have been necessary. A process of this kind requires either the transfer of the device layer of an SOI wafer to the glass wafer, which has proved extremely troublesome in the past [127] or the use of Chemical Mechanical Polishing (CMP) to thin the silicon layer post-bonding. Glass wafers with a Total Thickness Variation (TTV) of less than 15 μm could not be obtained. Thinning a silicon wafer down to a thickness of 10–20 μm when it is bonded to a glass wafer with a 15 μm TTV is bound to result in a very non-uniform thickness silicon layer; the silicon is likely to be polished through in places. And even if the layer transfer problem is resolved the issues of growing or



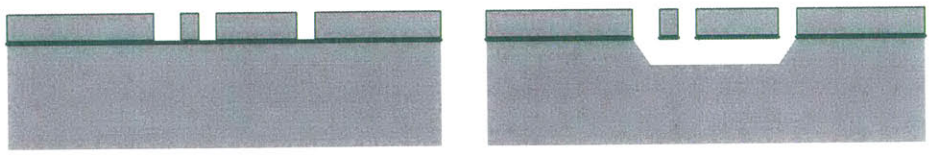
(a) A thinned silicon wafer bonded to a glass wafer that has been etched to create a stiction preventing relief.

(b) Thinned silicon wafer etched to create a suspended structure.

Figure 5-1: Device cross sections for a silicon-glass bonded wafer process. Unfortunately, the TTV of the available glass wafers is too large for reliable thinning of the silicon layer.

depositing a dielectric for the zipper actuator and of exposing bare silicon for electrical contact remain.

Processes where the device layer structure is undercut isotropically by xenon difluoride (XeF_2) or anisotropically by KOH were also considered, but the masking could not be made to work. Both processes necessitate holing the buried oxide without removing the oxide on the sidewalls of the device layer structure (Figure 5-2). This type of mask could possibly be fabricated starting from oxide layers of well chosen thicknesses or with a buried silicon nitride (rather than oxide) layer, but there will always be concerns about proper coverage of the corners, and in the end it was decided to minimize development risk. Considering the process integration issues that arose even despite the best efforts, that was a wise decision.



(a) The buried oxide must be holed without damaging the oxide on the device layer sidewalls

(b) Once the buried oxide is holed, a anisotropic etch could be used to relieve the device layer structure

Figure 5-2: Device cross sections for a undercut process illustrating the difficulty of protecting the sidewalls of the device layer structure while simultaneously holing the buried oxide.

5.1 Fabrication Process 1.0

The four mask variable capacitor fabrication process summarized in Figures 5-3 and 5-4 produces a fully KOH notched suspended device layer structure with bare silicon pads suitable for wire bonding. Highly doped (5–18 mΩ-cm) p-type 100 mm diameter SOI wafers with device and handle layer thicknesses of 20 μm and 300 μm respectively and 1.5 μm of buried oxide were supplied by Silicon Quest International (SQI) of Santa Clara, CA. Wafers with 10 μm thick device layers were also processed, but none survived; they were from a bad lot and very fragile, but there is no reason to believe good wafers with 10 μm device layers could not survive this process. Appendix A.3 contains a complete description of the fabrication process, as submitted to MIT's Microsystems Technology Laboratory Process Technology Committee.

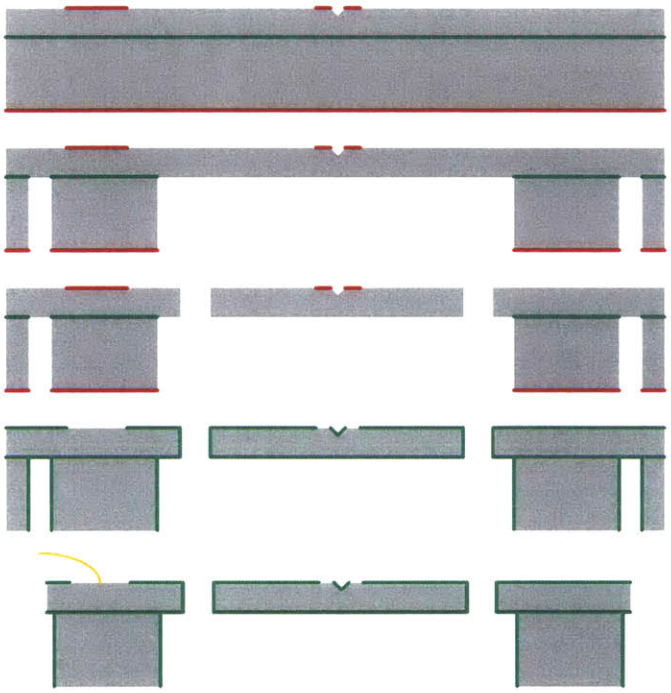
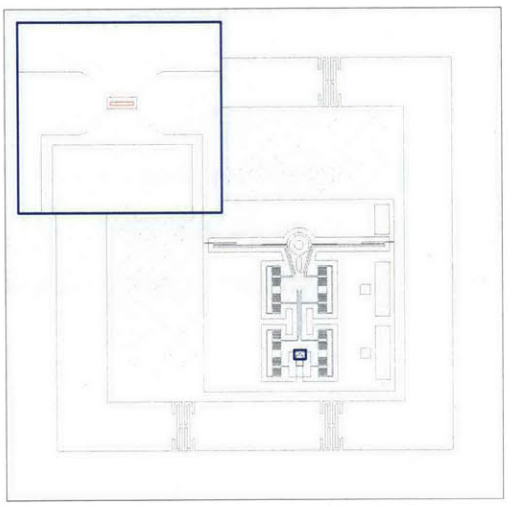
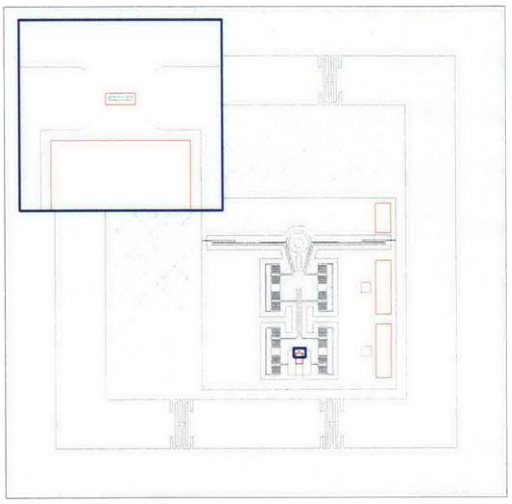


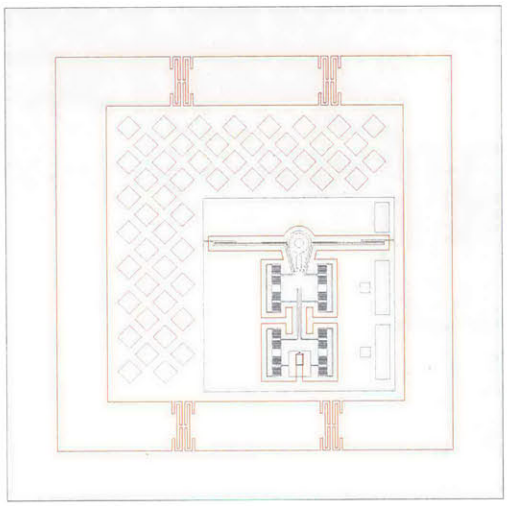
Figure 5-3: Variable capacitor fabrication process. Die level views of the masks are in Figure 5-4



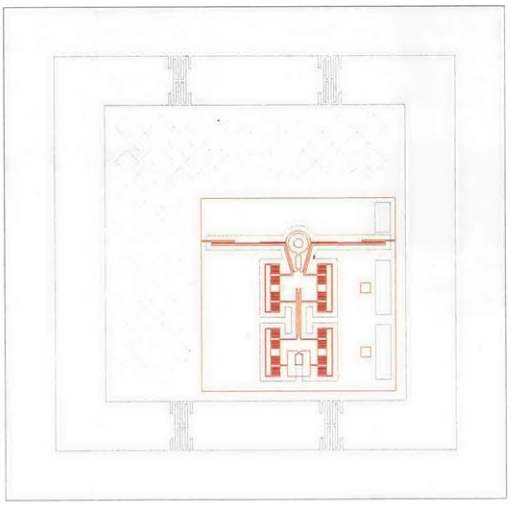
(a) Mask A: Nitride mask for KOH etch. Detailed view of the specimen inset.



(b) Mask B: Nitride mask for contact diffusion barrier. Detailed view of specimen inset.



(c) Mask C: Handle layer DRIE mask.



(d) Mask D: Device layer DRIE mask.

Figure 5-4: Die level views of the four process 1.0 masks. The geometry for each mask is shown in red, with the geometry of the other masks in gray for reference.

5.1.1 First Nitride Mask & KOH Etch

The first nitride mask (Mask A, Figure 5-4(a)) is used to etch through 150 nm of Low Pressure Chemical Vapor Deposited (LPCVD) silicon nitride. OCG 825 20CS photoresist from Arch Chemicals of Norwalk, CT masks the nitride during a 66 second CF_4 Reactive Ion Etch (RIE). The patterned nitride then serves as a hard mask for a KOH etch to create specimen notches and alignment marks.

KOH was employed to notch the specimens rather than the Focused Ion Beam (FIB) because the surfaces produced by FIB notching, while smooth, are not perpendicular to the wafer plane. Perpendicularity to the wafer plane is of no great importance for many applications, including capacitance, but it is important for this implementation. Chapter 4 established the importance of pull-in as well as the result that pull-in separation is determined by the relative magnitudes of the spring and capacitive forces. While the device structure has been stiffened in-plane, it remains rather compliant out of plane. This compliance is a natural consequence of the structure's in-plane extent, which is in turn an outgrowth of its moment attenuation duties (Chapter 2), but it leaves the device vulnerable to an out of plane pull-in effect if the fracture surfaces are not be normal to the wafer plane.

5.1.2 Second Nitride Mask & Diffusion Barrier for Contacts

After the KOH etch and subsequent clean, OCG 825 20CS resist is deposited and masks the same nitride layer for a second RIE to define electrical contact pads (Mask B, Figure 5-4(b)). The mask is dark where the contact pads will be, so the nitride there is not etched and can serve as a diffusion barrier during a later thermal oxidation step.

Resist is also left around the specimen notch. This does not protect the notch from oxidation because there is no nitride in the trench. It does, however, protect the notch from the RIE nitride etch, which might otherwise damage it. A consequence is that a small area surrounding the notch is left coated with nitride.

5.1.3 Handle Layer Mask & First DRIE Etch

The handle layer is DRIE'd (Mask C, Figure 5-4(c)) with an AZ P4620 resist from Clariant Corporation of Somerville, NJ and the buried oxide layer as an etch stop. The etch must be watched carefully to ensure it does not burn through the oxide and damage the underlying device layer. The etch removes the material behind what will become the device layer structure, creates the breakout tabs that will be used to singulate the wafer, and makes vias for the die attach compound. After the etch, a long Buffered Oxide Etch (BOE) removes the newly exposed buried oxide.

5.1.4 Device Layer Mask & Second DRIE Etch

The device layer etch (Mask D, Figure 5-4(d)) is the most challenging step of the fabrication process. It was determined through extensive experimentation that two coats of OCG 825 20CS resist (Appendix A.7) is the best way to mask the etch. Even when deposited at a very low spin speed, a single coat of OCG 825 20CS burns before the pattern is fully etched and the thicker resists (AZ P4620 and AZ P9260) do not hold small (3 μm) features sufficiently well. Great care is taken, but some die on the periphery of the wafer are invariably unevenly coated with resist due to surface variations in the device layer membranes. The etch is a special non-multiplexing recipe (STShall) that produces smooth, almost vertical (reportedly 89°) sidewalls. This etch defines the device layer structure: flexure, specimen, and actuator. Spin coating the resist in this step is the single biggest yield problem in the process.

5.1.5 Dielectric Deposition and Patterning

A 300 nm layer of thermal oxide is grown on the device to act as a dielectric for the zipper actuator. Without the dielectric, the zipper would electrically short and destroy itself. Thermal oxide was chosen because of firsthand knowledge of Li's [81] positive experience with it and because it was identified in the literature [24] as the most appropriate choice for a surprisingly challenging application, on par with a transistor's gate oxide. After the oxidation, a brief etch in 1:1 BOE:H_2O removes

a layer of oxynitride that has formed on the surface of the silicon nitride regions (and about 35 nm of oxide). A 45 minute dip in hot phosphoric acid then removes all nitride from the wafer, leaving bare silicon exposed at select locations for electrical contact. An experiment with legacy two stage devices determined the phosphoric acid does not damage the KOH notches. Employing nitride as a diffusion barrier for thermal oxidation is a variation on a well-established microfabrication process, Local Oxidation of Silicon (LOCOS) [77, 25].

5.1.6 Die Singulation

The die are separated from the wafer by fracturing tabs fabricated into the handle layer (Figure 5-5) or by cutting the tabs with an excimer laser. The tabs are 1 mm long, 50 μm wide, and haloed to prevent excessive thinning during their fabrication. Tabs were used instead of the die-saw out of concern for the fragile device layer structure.

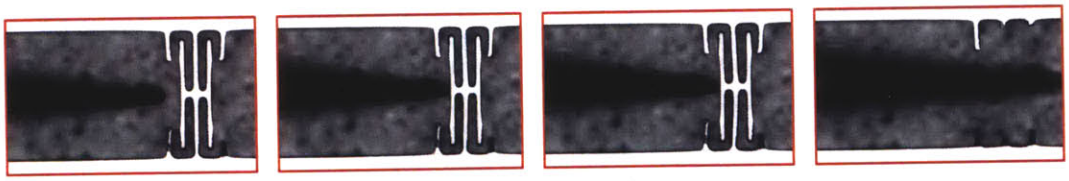


Figure 5-5: A sequence of micrographs of a tab being broken with an external probe.

Fracturing the tabs was a mixed success. Properly etched tabs fracture readily, but tend to create a large number of particles, that though they never resulted in the loss of a device, certainly have the potential. Cutting the tabs with an excimer laser, though some material is re-deposited on the surface of the die (Figure 5-6), is a much cleaner solution. Severing the tabs with a laser also has the advantage of being a non-contact process. Despite the use of a porous vacuum chuck from New Way Precision of Aston, PA, die tend to move substantial distances upon fracture of their final tab.

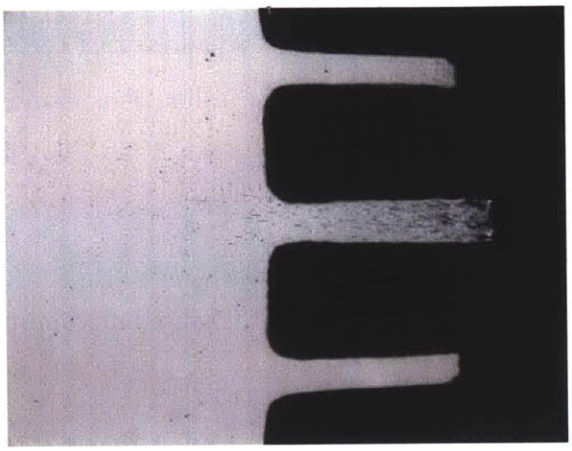


Figure 5-6: A tab cut with an excimer laser. Note the material re-deposition radiating out from the cut.

5.1.7 Assembly, Wire Bonding, and Sealing

After singulation, the die are shipped to Golden Altos Corporation of Milpitas, CA, where they are bonded into twenty-four pin single sidebraze packages from either Kyocera of Kyoto, Japan or NTK of Nagoya, Japan (part numbers KD-78382-G-1 and IDK24F1-167MAL respectively). A silver filled polymer die attach compound, JM7000, from Ablestik of Rancho Dominguez, CA is painted on the gold coated die cavity in an L-shape corresponding to the epoxy holes in the die (Figure 4-25). The die are then pressed into the JM7000, which flows up into the holes.

Also at Golden Altos, the die are connected to the package with aluminum wire as shown in Appendix B.1. Two wire bonds are used for many connections to enable estimation of the contact resistance. The size of the specimen anchor, which is also the specimen bond pad, is minimized to limit its parasitic capacitance.

After the specimens are fractured, the packages are returned to Golden Altos to be sealed in an inert nitrogen ambient (Figure 5-8(a)). The lid, HRC-372-21-50MT/100 GKL from Semi-Alloys Company of Mount Vernon, NY, has a glass window, which allows the movement of the zipper to be observed. Sealing is necessary for proper performance of the zipper actuator [23]; in air, there is a cycle to cycle increase in the operating voltage and electrostatic stiction.

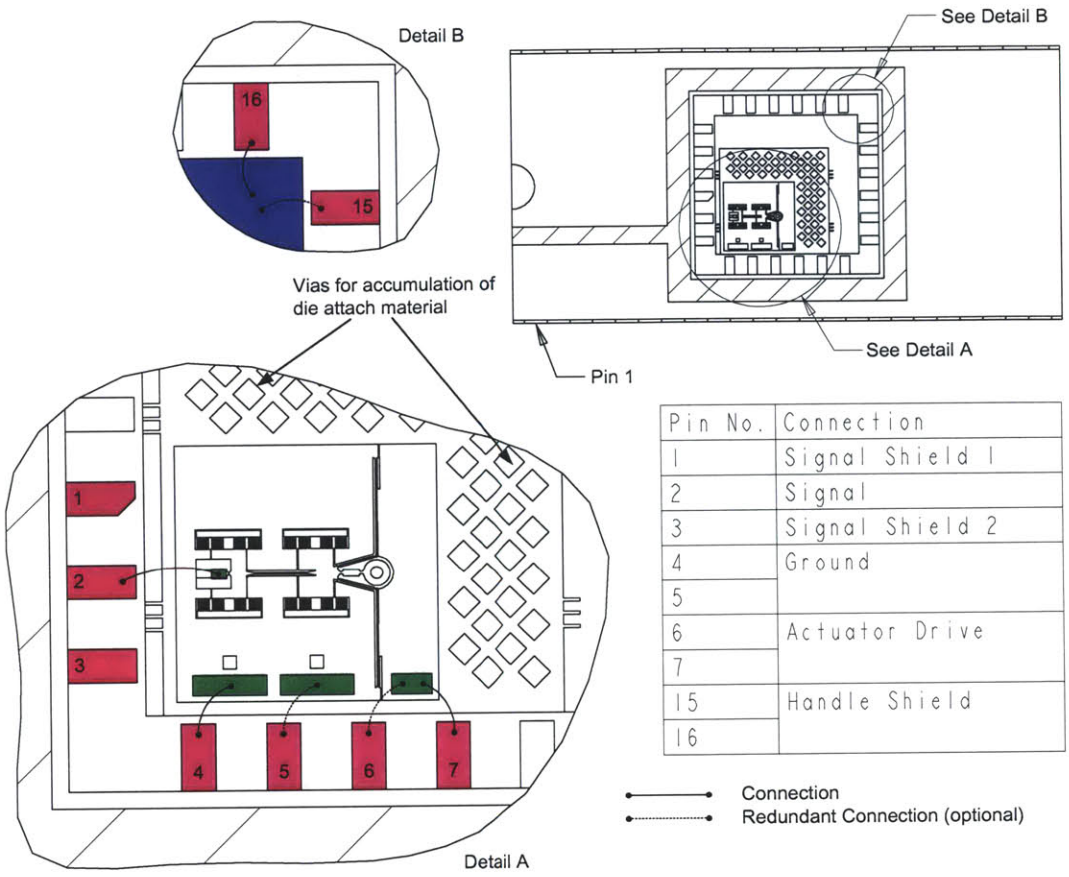


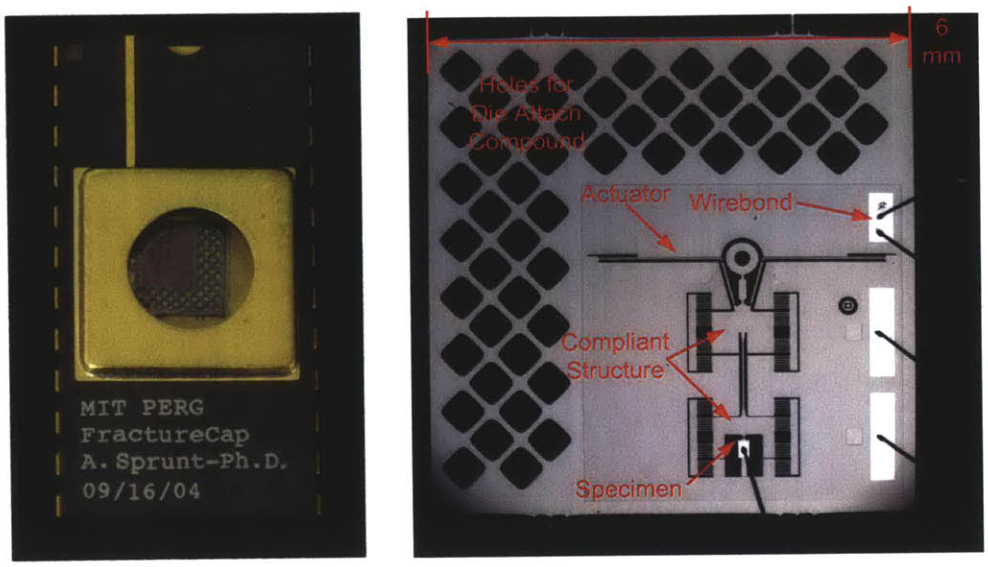
Figure 5-7: Variable capacitor wire bonding diagram

5.2 Testing the First Prototype

The successes of the first prototype include the fabrication of the zipper actuators and specimens. The principal disappointment was a failure to detect any capacitance change when the structure is actuated with the zipper, or even manually with a probe. This as well as an unanticipated coupling between the actuation signal and capacitance measurement signal are the result of three different problems: poor fracture performance, specimen sideslip, and poor handle layer electrical contact.

5.2.1 Zipper Actuators

Functioning zipper actuators were fabricated, but it is necessary to drive them with an amplitude modulated square wave (Figure 5-9) and to seal the package to prevent



(a) Sealed

(b) Die-level

Figure 5-8: First variable capacitor prototypes

the various stiction and drive voltage effects described in [23]. Sealing the package was contemplated during the design of the device, so its necessity is considerably less inconvenient than might have otherwise been the case.

5.2.2 Fracture Specimens

Inadvertent breakage of specimens during the fabrication process is a much smaller problem than initially feared. After the handle layer etch creates device layer membranes, the wafers are handled with extreme care. Methanol drying is used whenever possible, spin-rinse dryers are not used at all, and bubbling wafer baths are avoided. About 10% of the specimens are nonetheless broken, but this level of breakage is not nearly as bad as had been feared. The fracture results discussed in the following sections are all the result of deliberate fracture with an external probe.

5.2.3 Fracture Problem

None of the specimens fractured as intended. Instead of fracturing along the (110) plane normal to the wafer surface, the vast majority of specimens fracture by eject-

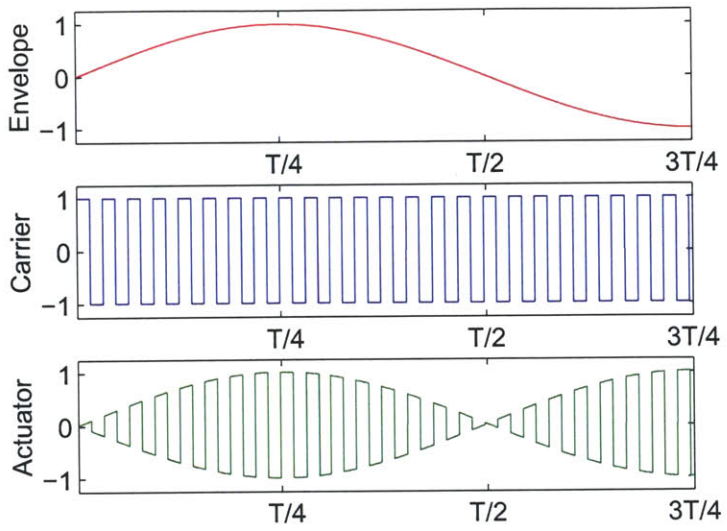


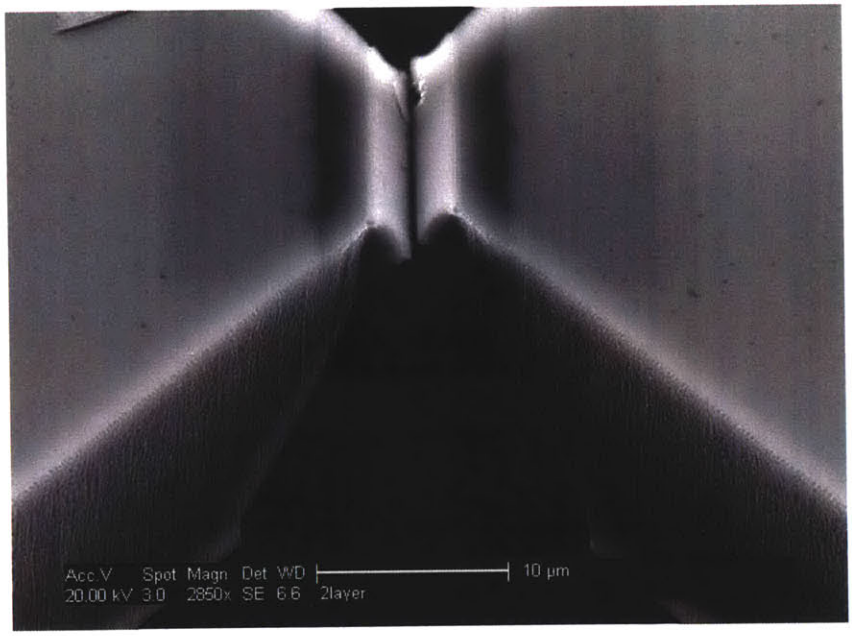
Figure 5-9: The zippers are driven with an amplitude modulated square wave to prevent electrostatic stiction. The sine wave envelope cycles the zipper on and off, while the square wave carrier prevents charge from accumulating on the electrodes, especially in a humid ambient.

ing a wedge of material bounded by (111) planes (Figure 5-10(a)), with a minority fracturing along (111) plane(s) (Figure 5-10(b)) without material ejection.

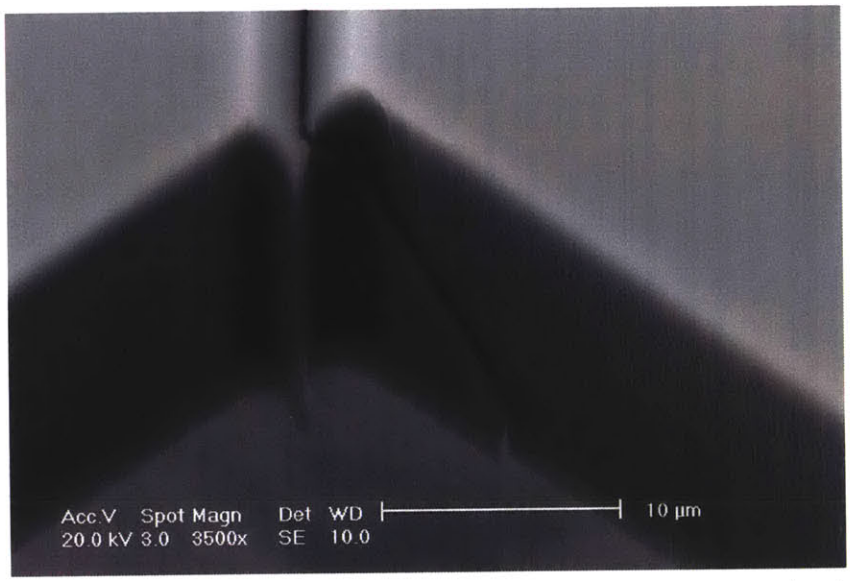
The problem was traced to the thermal oxidation step and attributed to a process similar to the oxide sharpening [91, 90, 69, 119] commonly used to make AFM tips. Thermal oxidation sharpens features with small included angles, e.g. AFM tips, but is reported to blunt those with large included angles, e.g. trenches or notches. It is thought this blunting results in higher fracture forces and material ejection or fracture surfaces that are not perpendicular to the wafer plane.

No capacitance change could be detected in the specimens that ejected material, because the change in capacitance from separating a pair of lines is so much smaller than the change from separating a pair of planes. No capacitance change could be detected from the specimens that did not eject material because of a concurrent sideslip problem discussed in Section 5.2.4.

Even without the sideslip problem, it is important that the fracture be normal to the wafer plane, because if it is not, a second pull-in mode could be exhibited. In the first pull-in mode, the gap between the fracture surfaces collapses as the surface



(a) A member of the majority of specimens that ejected a wedge of material when fractured. This reduces the capacitor from a pair of planes to a pair of lines.



(b) A member of the minority of specimens that fractured along the (111) plane rather than the (110) plane as was expected. It could have been used as a capacitor but for the sideslip (Section 5.2.4), though there probably would have also been problems with out of plane pull-in.

Figure 5-10: Fractured specimens from the first prototype.

attached to the flexure moves in the y-direction (as defined in Figure 4-25). If the fracture surface does not track the (110) plane, which is parallel to the xz-plane, a second mode exists, where the gap can collapse due to the motion of the flexure in the z-direction. The flexure is much more compliant in this out of plane direction, causing an increase in the minimum stable gap. Similar reasoning precludes the use of FIB notched specimens.

5.2.4 Specimen Sideslip

Due to relative motion between the two fracture faces, no capacitance change is detectable in the specimens that did not eject material. This motion would not have been of great importance if the fracture faces were perfectly flat, but because the specimens are all 20 μm thick, the fracture faces are merely complementary. When the faces shifted, asperities on their surfaces are no longer aligned, and the gap does fully close. The specimens are typically "stuck" open by approximately 200 nm (Figure 5-11).

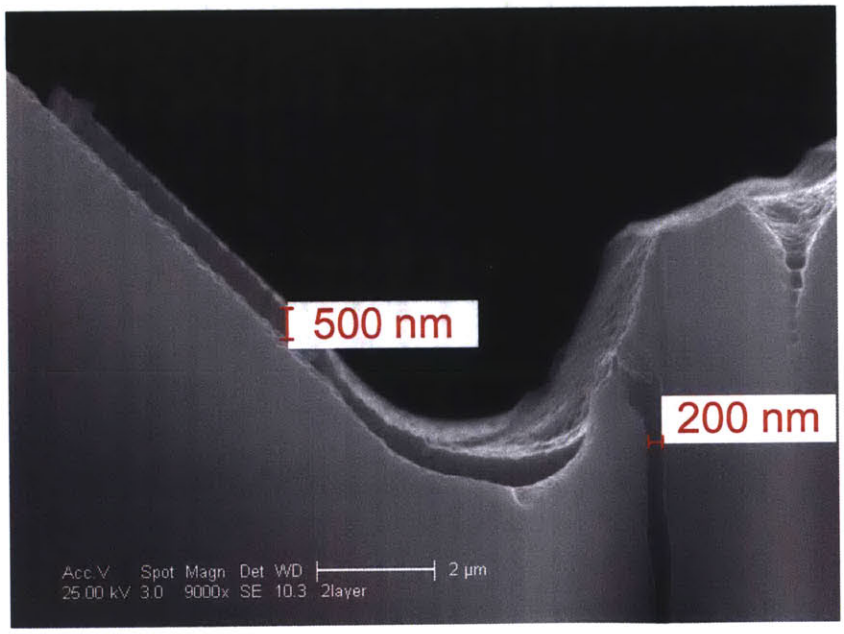


Figure 5-11: The two halves of a variable capacitor "stuck" open because asperities on the fracture surfaces are no longer properly aligned.

A minimum gap of 200 nm places capacitance change well out on the flat part of the capacitance-distance plot (Figure 4-10). A small change may have been seen when the device is actuated manually with a probe, but the difference in the output from the capacitance measurement circuit (Section 5.2.6) is in the millivolt range, and therefore equivocable.

The source of the sideslip is the force applied to the specimen anchor by the wire bond (Figure 5-12). The bond wire is under tension, and pulls ever so slightly on the cantilevered specimen anchor to produce approximately 500 nm of sideslip. The amount of sideslip is consistent with a beam theory based prediction of the deflection based on the break force of the wire bond. The design error of locating the wire bond at the end of a cantilever beam was magnified by the beam being thinner than drawn due to taper in the handle layer etch. Experimentally, the sideslip is not present in die that have not been wire bonded. See Section 5.3.2 for the solution to this problem.

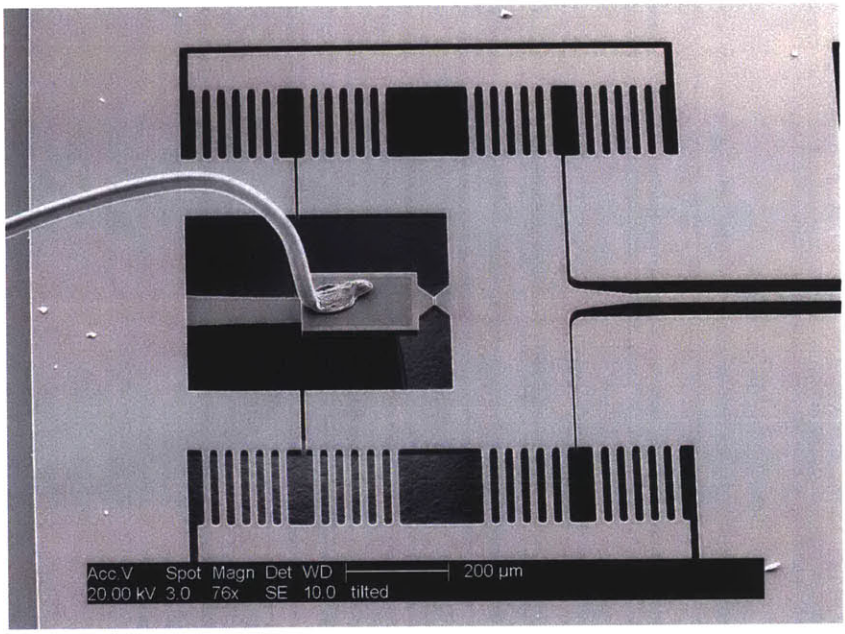


Figure 5-12: The specimen stage and anchor of a variable capacitor. Note the wire bond running from the specimen anchor.

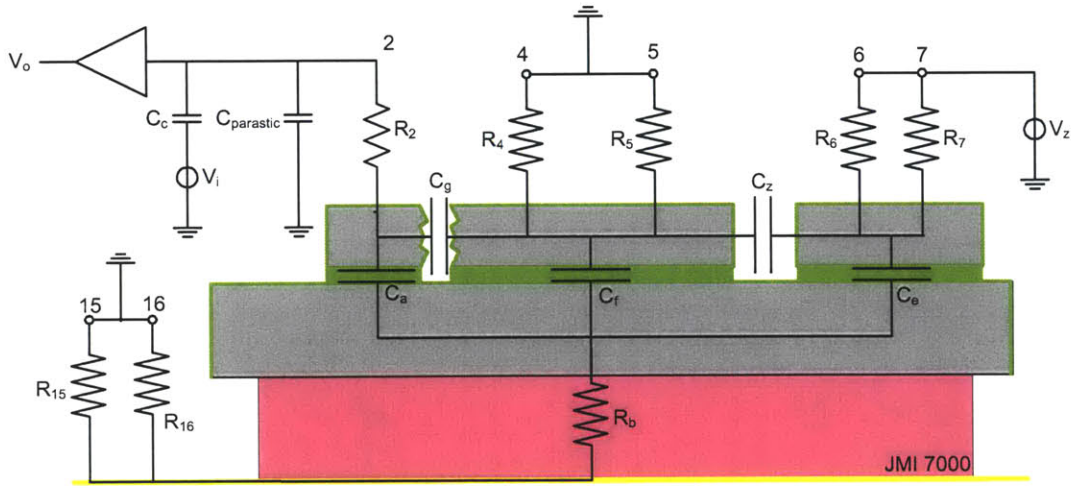


Figure 5-13: Variable capacitor circuit diagram

5.2.5 Crosstalk

Figure 5-13 is a circuit diagram of the variable capacitor. The anchor side of the specimen is connected to the capacitance measurement circuit through pin 02. Pins 04 and 05 ground the flexure side of the specimen to facilitate measurement of the capacitance and to provide a reference voltage for the actuation signal to work against. The zipper actuation signal is applied through pins 06 and 07. Pins 15 and 16 are connected to the handle layer (through the gold at the bottom of the die cavity and the JM7000 silver filled adhesive), so it can be driven as a shield to reduce parasitic capacitance, or at least be grounded to prevent crosstalk.

Unfortunately, the resistance, R_b, of the bond connecting the die to the package is much larger than expected. Rather than being a few ohms, it is most likely in the hundreds of ohms range (Figure 5-14). The model to formulate that estimate is based on the circuit in Figure 5-15 and is implemented using Kirchhoff's Current Law to produce a set of equations for the current at each node:

$$P\mathrm{j}\omega e = G_{internal}e + G_{external}v, \tag{5.1}$$

where P is the capacitance matrix, L is is the conductivity matrix, R is the matrix of

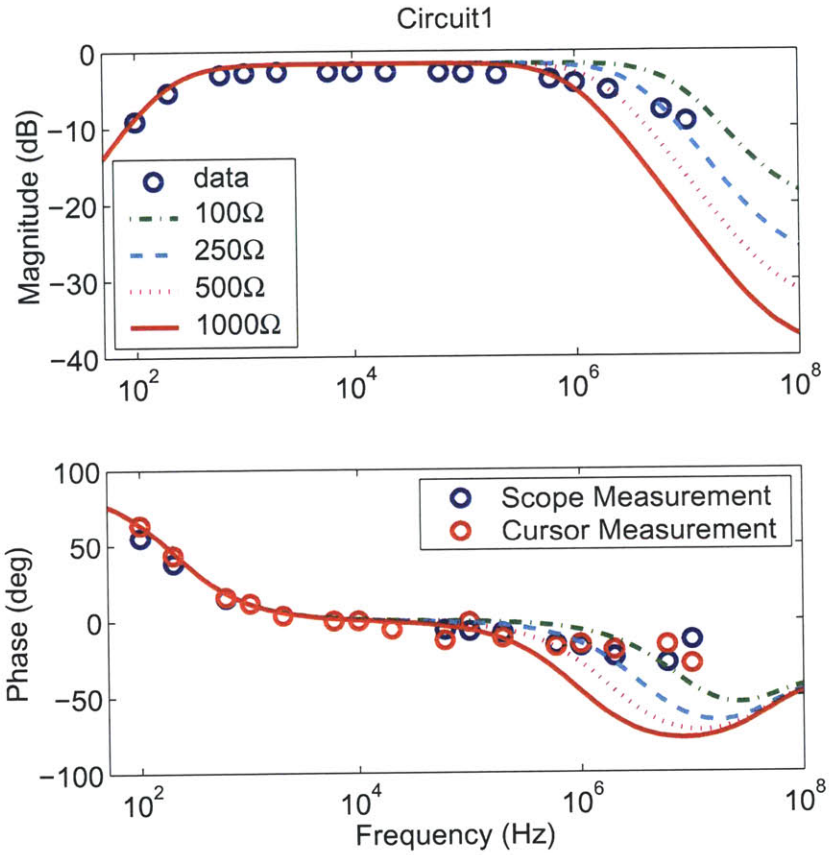


Figure 5-14: Bode Plot of variable capacitor testing results. For this test: pin 02 floats, pin 04 is grounded, the output of pin 06 is measured, and pin 15 is driven.

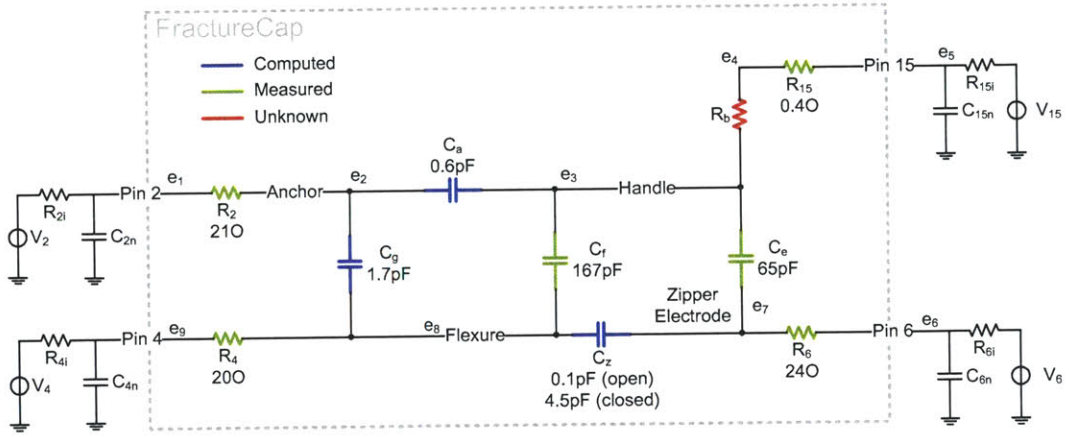


Figure 5-15: Variable capacitor circuit model. R_{xi}, C_{xn}, and V_x are altered to reflect the test boundary conditions as necessary.

input impedances, e is the vector of voltages at each node, v is the vector of external potentials, ω is the excitation frequency in $\frac{\text{radians}}{\text{s}}$, and j is $\sqrt{-1}$. Solving for the voltage at each node,

$$e = (P\mathrm{j}\omega - L)^{-1} Rv. \tag{5.2}$$

Because the handle layer is not firmly grounded, the actuation signal, which is running between $\pm 200\,\text{V}$, is coupled through C_e and C_a into the capacitance measurement circuit. To correct this, the second prototype die are eutectically bonded to the bottom of the die cavity to reduce R_b.

5.2.6 Measurement Circuit Testing

Hongshen Ma designed a front-end amplifier circuit for measuring the capacitance of the fracture surfaces [86, 88]. A diagram of the circuit's conceptual topology (based on [12]) is in Figure 5-16. The variable capacitor, C_g, and the reference capacitor, C_2, form a capacitive divider. The parasitics, represented by capacitor C_3, are modelled in parallel with the variable capacitor. The AC output of the divider, V_d, when sinusoidally excited at 20–50 kHz by V_{in} is:

$$V_d = \frac{C_2}{C_g + C_2 + C_3} V_{in}. \tag{5.3}$$

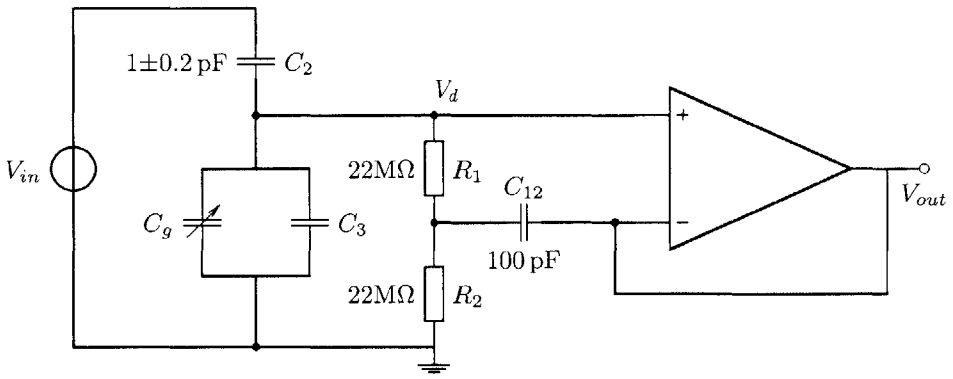


Figure 5-16: Conceptual circuit for capacitance measurement

A non-inverting operational amplifier buffers the signal, V_d. The network formed by R_1, R_2, and C_{12} sets the DC component of V_d and minimizes attenuation at the excitation frequency. A guard ring printed on the circuit board around the amplifier's non-inverting input minimizes parasitics. Within the excitation frequency range (20–50 kHz),

$$V_{out} = V_d. \tag{5.4}$$

A photograph of the board is in Figure 5-17. The device's sidebraze package fits directly into the board's blue socket. A detailed schematic of the board is in Appendix B.3.

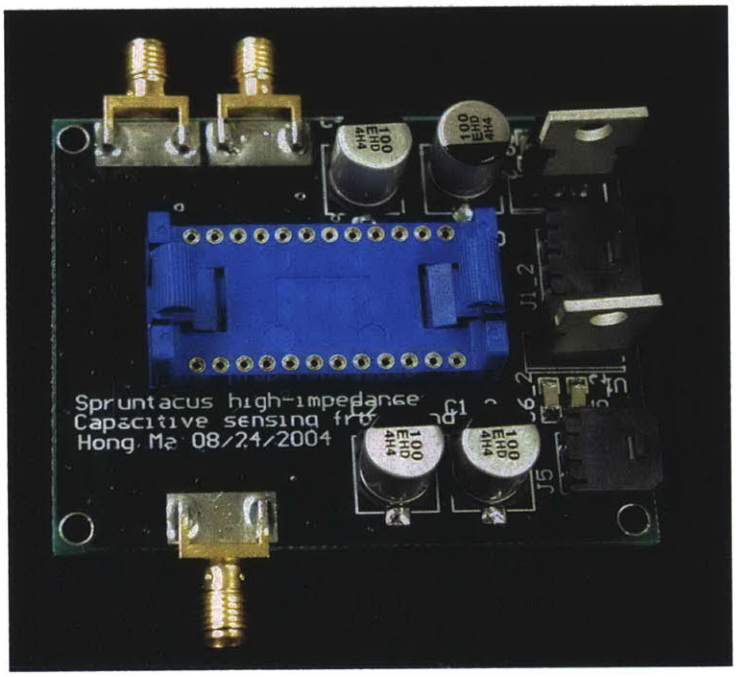


Figure 5-17: Capacitance measurement board. Note the blue socket for insertion of the variable capacitor package.

To test the measurement circuit, a series of small circuit boards with surface mount capacitors and wires soldered to them (Figure 5-18) are inserted into the socket in place of C_g. The output of the circuit, V_{out}, is plotted with respect to the capacitance of the boards as measured on an HP4192A LF Impedance Analyzer (Figure 5-19).

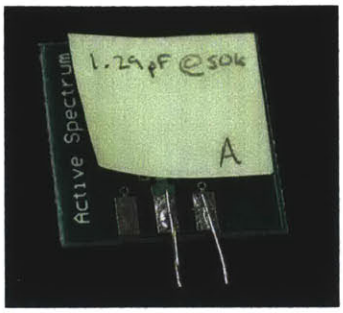


Figure 5-18: Small circuit board used as a capacitor

The size of the reference capacitor, C_2, and of the parasitics, C_3, are only roughly known; a model is fit to the data to determine their values. For the fitting program, a cost function,

$$F = \sum_{i=1}^{n} \left(V_{out,i} - V_{in} \frac{C_2}{C_{1,i} + C_2 + C_3} \right)^2, \tag{5.5}$$

where n is the number of data points, measures how far the data is from the model output. Gradient functions:

$$\frac{\partial F}{\partial C_2} = \sum_{i=1}^{n} \left[-2V_{in} \left(V_{out,i} - V_{in} \frac{C_2}{C_{1,i} + C_2 + C_3} \right) \left(\frac{C_{1,i} + C_3}{(C_{1,i} + C_2 + C_3)^2} \right) \right] \tag{5.6}$$

$$\frac{\partial F}{\partial C_3} = \sum_{i=1}^{n} \left[2V_{in} \left(V_{out,i} - V_{in} \frac{C_2}{C_{1,i} + C_2 + C_3} \right) \left(\frac{C_2}{(C_{1,i} + C_2 + C_3)^2} \right) \right], \tag{5.7}$$

give the derivative of the cost function with respect to the model parameters, C_2 and C_3, varied to minimize the cost function. The parameter estimation program based upon these equations (Appendix D.2) produces values of 1.07 pF for C_2 and 0.28 pF for C_3, which in turn yield model output that lines up well with the experimental data (Figure 5-19).

From the board's success measuring the capacitance of different circuit boards and our success in modelling the board's performance, it is concluded that the circuit is functioning properly and would have detected a change in capacitance had the specimens fractured as intended.

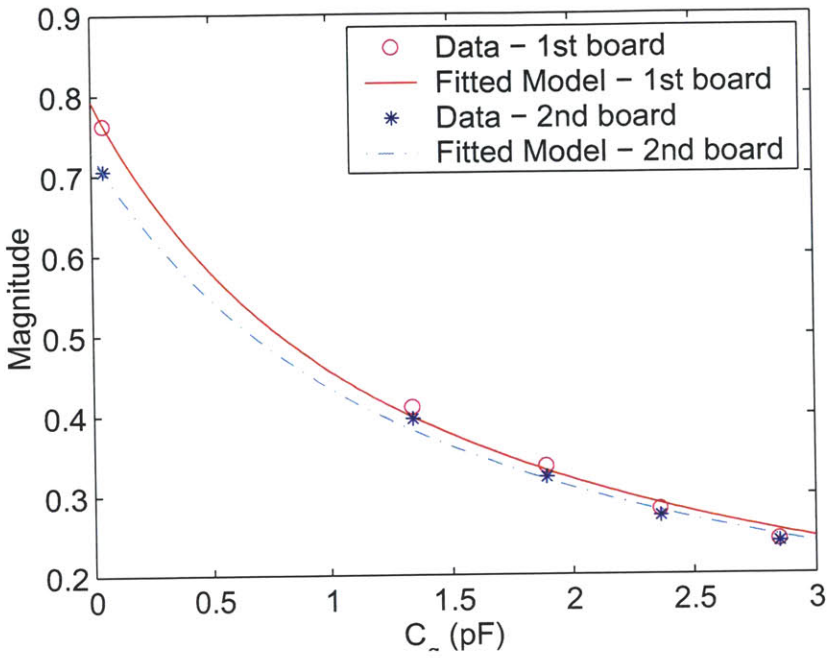


Figure 5-19: The results of the tests and the model fits. Two different versions of the board were fabricated, differing only in the pin-out of the variable capacitor package.

5.3 The Second Prototype

The main changes to the variable capacitor design for the second prototype, a nitride cover for the notch during thermal oxidation, the relocation of the wire bond contacts, and eutectic assembly, are responses to the problems with the first prototype, but several other small changes have also been made. Among the lesser changes, those made to the zipper are motivated by observations of the first prototype's performance or the design optimization described in Section 4.5.

5.3.1 Specimen Nitride Cover

After the notch is etched with KOH, a silicon nitride cap is deposited over it for protection during thermal oxidation. As with the nitride covers over the areas that will become electrical contacts, the specimen nitride cover prevents thermal oxidation (and therefore blunting).

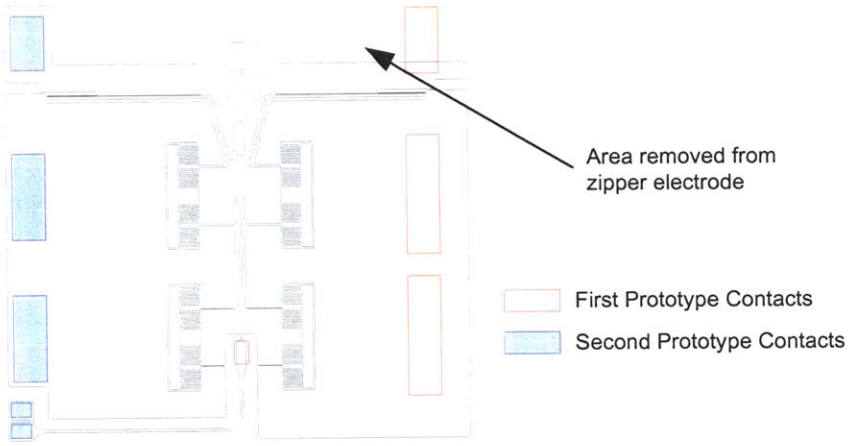


Figure 5-20: The second prototype device layer geometry with the first prototype contacts overlaid.

5.3.2 Bond Pads Relocated

The bond pads (especially the pad on the specimen anchor) are moved to stiffer portions of the structure close to where it is bonded to the die cavity (Figure 5-20). FEA confirms the new contact locations result in sub-nanometer displacement of the fracture surfaces.

5.3.3 Zipper Geometry Changes

Based on the optimization described in Section 4.5, the zipper beam height is increased from 20 μm to 30 μm, and the stroke is decreased from 9 μm to 3 μm. Reducing the stroke also removes a discontinuity from the zipper's motion. In the first prototype the gap between the zipper and the electrode is a constant 4.5 μm for the length of the starting zone cantilever, and then increases steadily to 9 μm at the far end of the zipper. The slope discontinuity between the constant-gap zone and the increasing-gap zone produces a hesitation that is eliminated by changing to a constant 3 μm gap.

Other changes include thinning the starting zone cantilever from 10 μm to 7.5 μm to reduce its stiffness by approximately one half, with a corresponding difference in starting voltage and reducing the area of the zipper electrode bonded to the buried oxide, to decrease the size of C_e, and thereby decrease the strength of the coupling

between the actuator and the capacitance measuring circuit.

5.3.4 Specimen Types

Based on the limited results obtained from the first prototype, the specimens for the second prototype are slightly revised: 5 μm, 10 μm, and 15 μm straight specimens, 10 μm hourglass specimens, and 10 μm double straight specimens. The population of straight specimens is increased because of their relative success in the first prototype. The straight specimens are more easily fabricated, and though they did not produce good fracture surfaces, they failed in the same manner as the hourglass type specimens.

5.4 Fabrication Process 2.0

The second version of the fabrication process is outlined in Figure 5-21 and completely described in Appendix A.4. The most significant change is the addition of nitride deposition and patterning steps after the KOH etch. With this deposition, the notches are covered during thermal oxidation, eliminating any oxide blunting effect. The literature confirms a nitride cap prevents oxidation on (111) planes [132]. There may be some strain induced lattice damage near the nitride boundary [14], but no ill-effects attributable to such damage are observed.

Unfortunately, circumstances dictated the fabrication process could not be executed exactly as intended. A substantial upgrade of the DRIE equipment was scheduled for shortly after fabrication of the first prototype was completed. Bringing the handle layer etch under control consumed a considerable amount of time and several wafers, so it was decided to etch the handles of the entire stock of wafers before the machine's characteristics were altered by the refurbishment.

Working from non-virgin wafers necessitates altering the ideal fabrication process to that seen in Figure 5-22. A complete description of the process is in Appendix A.5. Working with wafers whose handle layers have already been etched limits design changes to the device layer and doubles the number of masking steps performed on

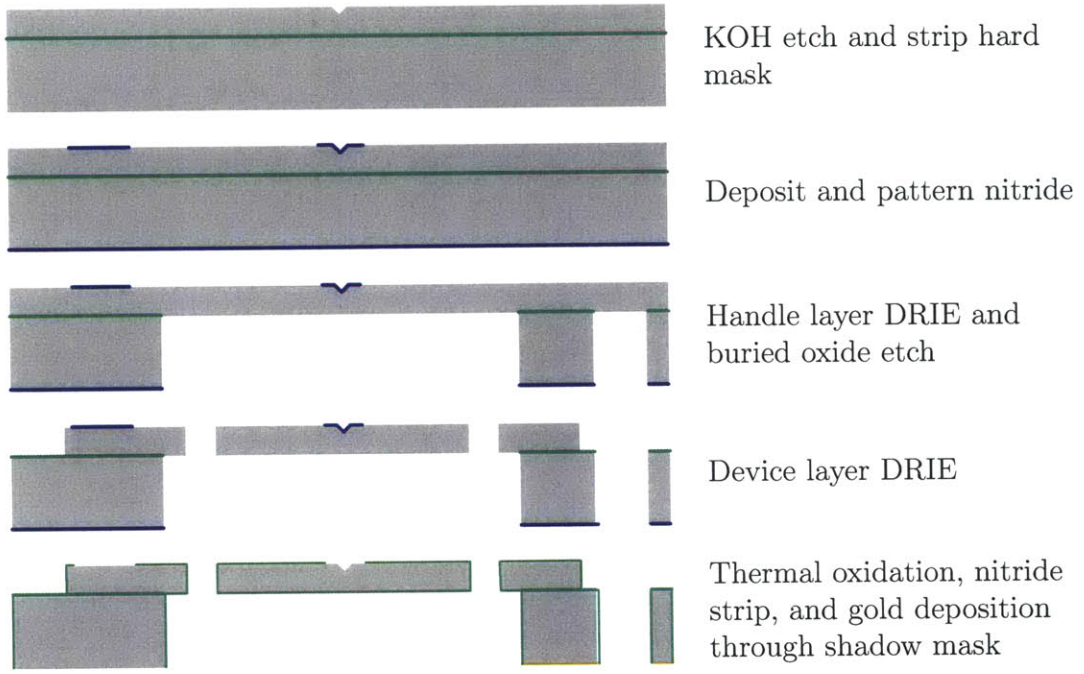


Figure 5-21: Variable capacitor fabrication process version 2.0. Note the KOH notch is covered with silicon nitride during the thermal oxidation.

device layer membranes.

5.5 Testing the Second Prototype

Poor fracture performance is the most significant problem with the first prototype, so determining the new devices' fracture characteristics is the focus of the first series of tests. Specimens from several different points in the fabrication process are fractured and analyzed with X-rays to determine the effect of oxidation and the nitride cap on the surfaces' fracture morphology.

5.5.1 Oxidized Specimens

SEM images of a typical specimen from the second version of the variable capacitor fabrication process are in Figure 5-23. The device shown was oxidized, stripped of nitride, and diced from the wafer, but not packaged (position B in Table 5.1). The

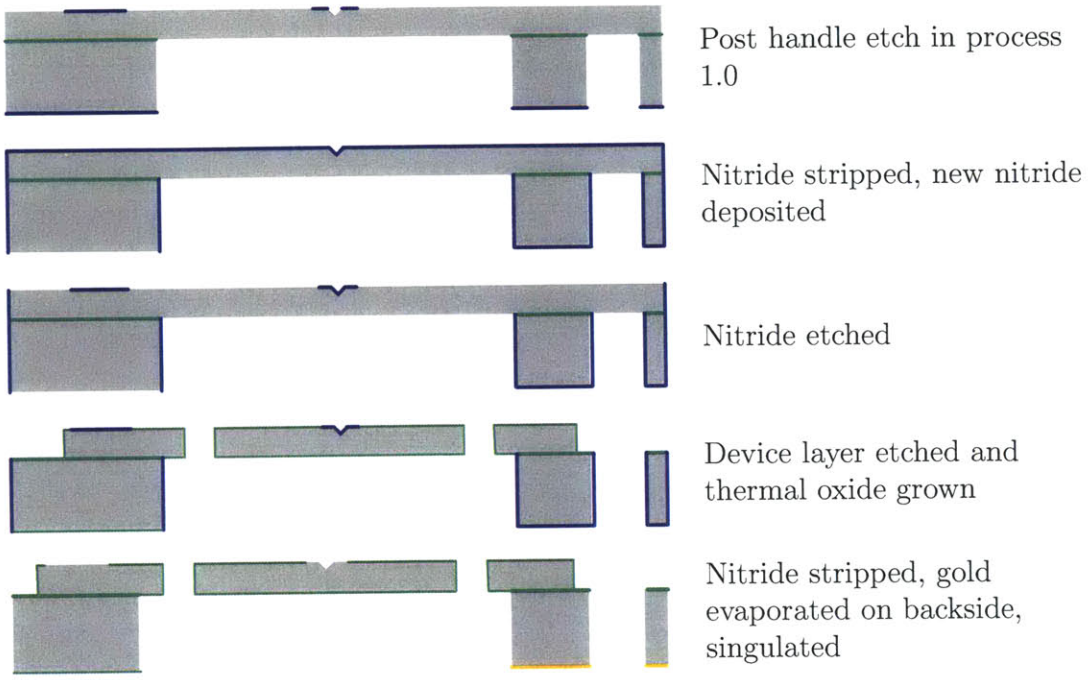
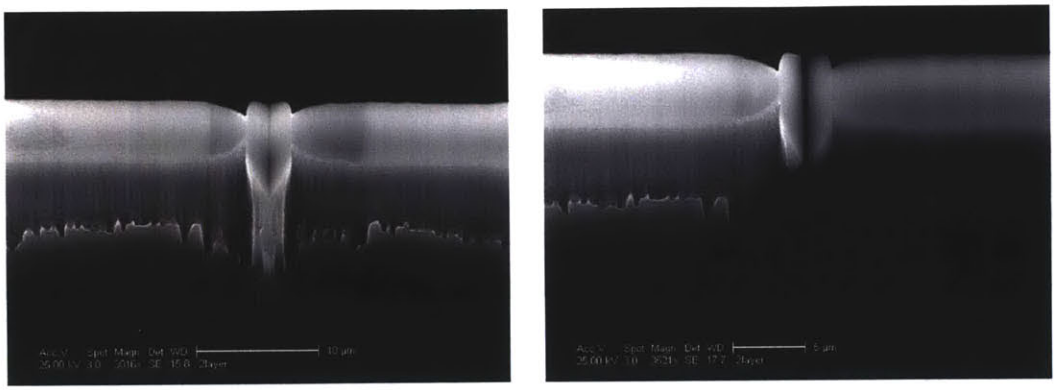


Figure 5-22: Variable capacitor fabrication process 2.0 altered for non-virgin wafers

brightness change around the notch (as well as a subsequent Energy Dispersive X-ray analysis, Section 5.5.3) indicates the notch was covered with silicon nitride during the oxidation process, and is now bare silicon. The upper half of the sidewalls are rougher than the lower half, because the resist broke down near the end of the etch, but that does not appear to have materially influenced the fracture behavior, which is essentially the same as that of specimens from the initial version of the fabrication process: ejection of material bound by the (111) planes originating at the tip of the notch.

5.5.2 Non-Oxidized Specimens

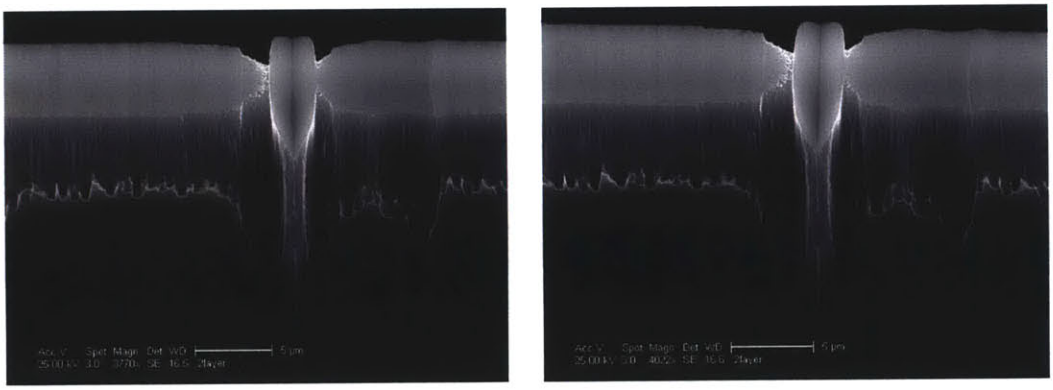
To determine whether the oxidation step is truly the cause of the material ejection, specimens from a wafer that had been through the entire fabrication process right up to oxidation were fractured (position A in Table 5.1). SEM images of a typical specimen are in Figure 5-24. Once again, the different brightness level of the region immediately surrounding the notch (as well as a subsequent EDX analysis) confirm



(a) Before (b) After

Figure 5-23: SEM images of the same second prototype before and after fracture. The notch was covered with nitride as intended during oxidation, but the material ejection problem persists. The die imaged here is equivalent to die 51 and 54 in the EDX section.

the notch has been covered with silicon nitride. The pre and post-fracture images appear identical because the specimen fractured very cleanly; a higher magnification image would reveal a 30 nm gap between the two surfaces.



(a) Before (b) After

Figure 5-24: SEM images of the same un-oxidized second prototype before and after fracture. The notch is still covered in nitride, but the fracture sufficiently perfect the fracture is not visible at this magnification. The die imaged here is equivalent to die 65 in the EDX section.

The fracture results from the non-oxidized devices place the problem with either the oxidation step or the nitride strip, but the nitride strip is an unlikely source because two-stage devices from the fracture development problem were deliberately exposed to hot phosphoric acid for the same amount of time, and went on to fracture

well.

5.5.3 EDX Results

An Energy Dispersive X-ray (EDX) analysis is conducted to determine if covering the KOH notches with silicon nitride had prevented their oxidation. Three fracture specimens from different points in the fabrication process (Table 5.1) are examined. Die 65 is extracted before thermal oxidation; die 51 and 54 are extracted after thermal oxidation and nitride strip.

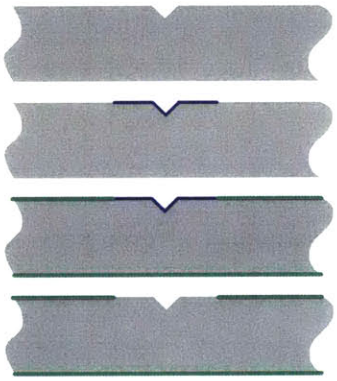
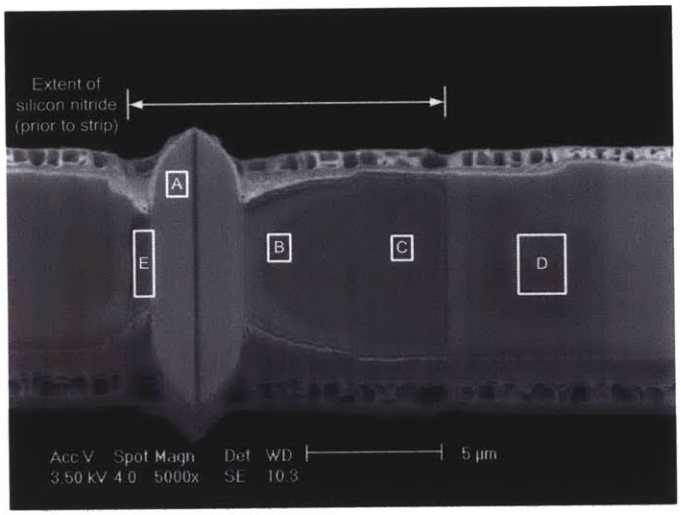
			KOH etch and mask strip Nitride deposition and patterning, DRIE sidewalls Thermal oxidation Nitride strip
A	die 65 (fractured)		
B	die 54 (un-fractured) & die 51 (fractured)		

Table 5.1: EDX analysis conducted on die from different points in the fabrication process.

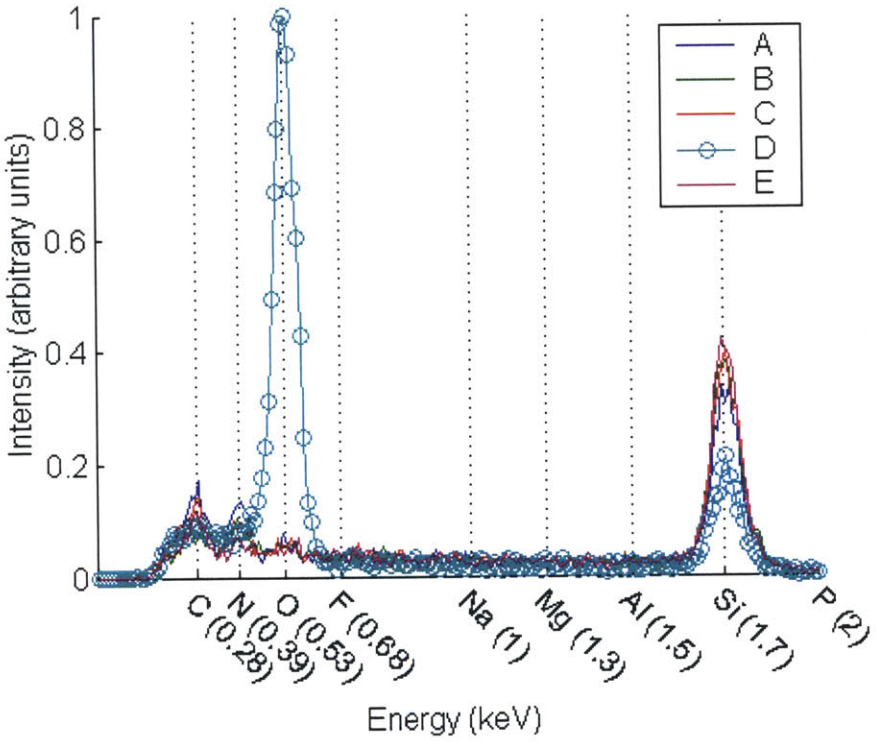
The spectra[1] (Figures 5-25 and 5-26) indicate no oxide was grown in the notch or the surrounding nitride coated area. Spectra at sites A, B, C, and E on die 54 and at sites F, G, I, and J on die 51 have no oxygen peak and a strong silicon peak consistent with bare silicon. The spectra at sites D and H have a strong oxygen peak and a weaker silicon peak consistent with a coating of thermal oxide. The carbon peak may be due to incomplete removal of the teflon deposited during DRIE, or it may be low-frequency noise; the data for die 51, taken later when the detector was cooler, exhibits a less pronounced peak.

The EDX derived element maps in Figures 5-27 and 5-28 confirm the absence of thermal oxide in the KOH trench and on the surrounding surface, as well as the

[1]The x-ordinate labels were derived from the wavelengths of the K-series X-ray transitions in [42, Table 777, p. 697]. The wavelengths, λ, were converted to energies with the equation $E = \frac{h_p c_p}{\lambda}$, where h_p is Plank's constant ($4.136 \cdot 10^{-15}$ eV sec) and c_p is the speed of light (299,792,458 $\frac{\mathrm{m}}{\mathrm{s}}$) .

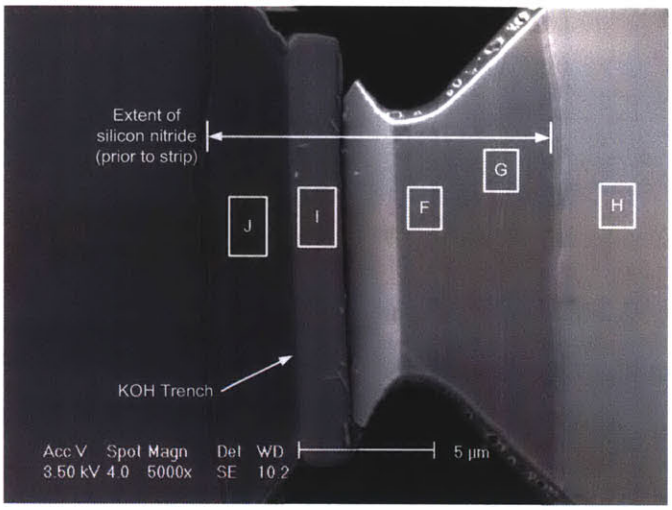


(a) Sample sites on die 54, left specimen: oxidized, nitride stripped, un-fractured

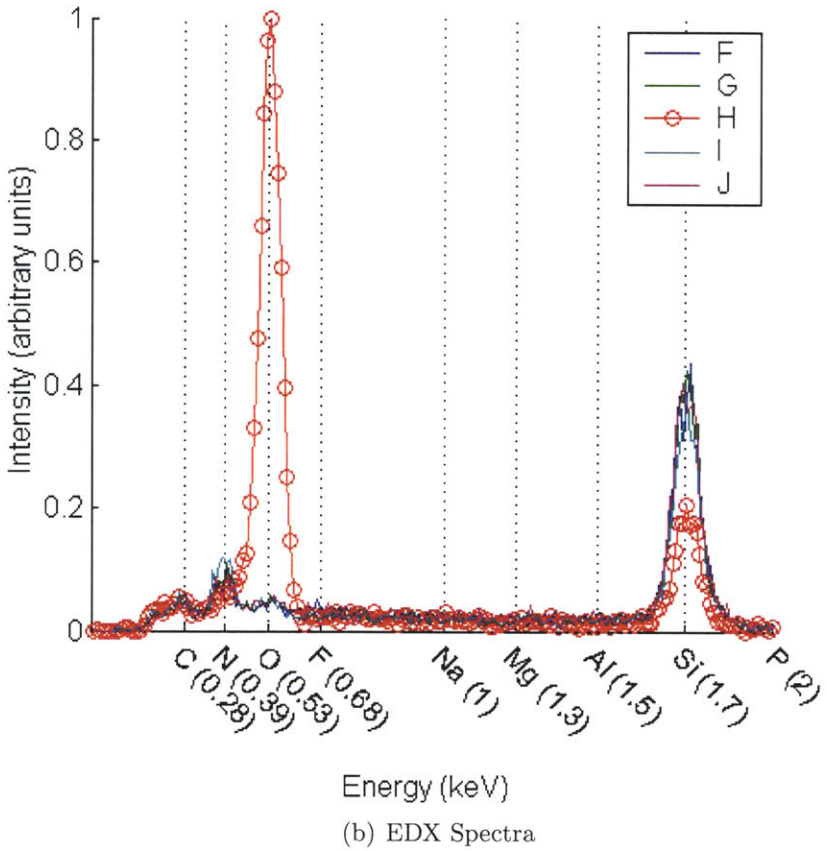


(b) EDX Spectra

Figure 5-25: EDX spectra for die 54. Note the strong solitary oxygen peak at site D indicating the presence of silicon oxide there, but not elsewhere on the specimen.



(a) Sample sites on Die 51: oxidized, nitride stripped, fractured



(b) EDX Spectra

Figure 5-26: EDX spectra for Die 51. Note the strong solitary oxygen peak at site H indicating the presence of silicon oxide there, but not elsewhere on the specimen.

presence of oxide outside the nitrided region. The nitrogen map in Figure 5-28 of die 65 from which the nitride had not been stripped confirms nitride layers are detectable by EDX analysis. The map of die 51 also illustrates the complementarity of the oxide growth with the nitrided region; the two fit hand-in-glove.

The evidence from fracturing oxidized specimens, fracturing non-oxidized specimens, and the EDX analysis indicates that though the thermal oxidation step is responsible for poor fracture performance, the oxidation process does not itself damage the KOH notches; the prolonged exposure to high temperature alone is enough to blunt the notch. The specimens fracture well prior to oxidation, and the nitride cover does protect the notches from oxidation, but post-oxidation, the specimens fracture poorly. Diffusional smoothing could explain these facts. At elevated temperatures, i.e. the 1050°C of a thermal oxidation step, the extreme sharpness of the notch results in a large driving force for diffusion to reduce the curvature [6].

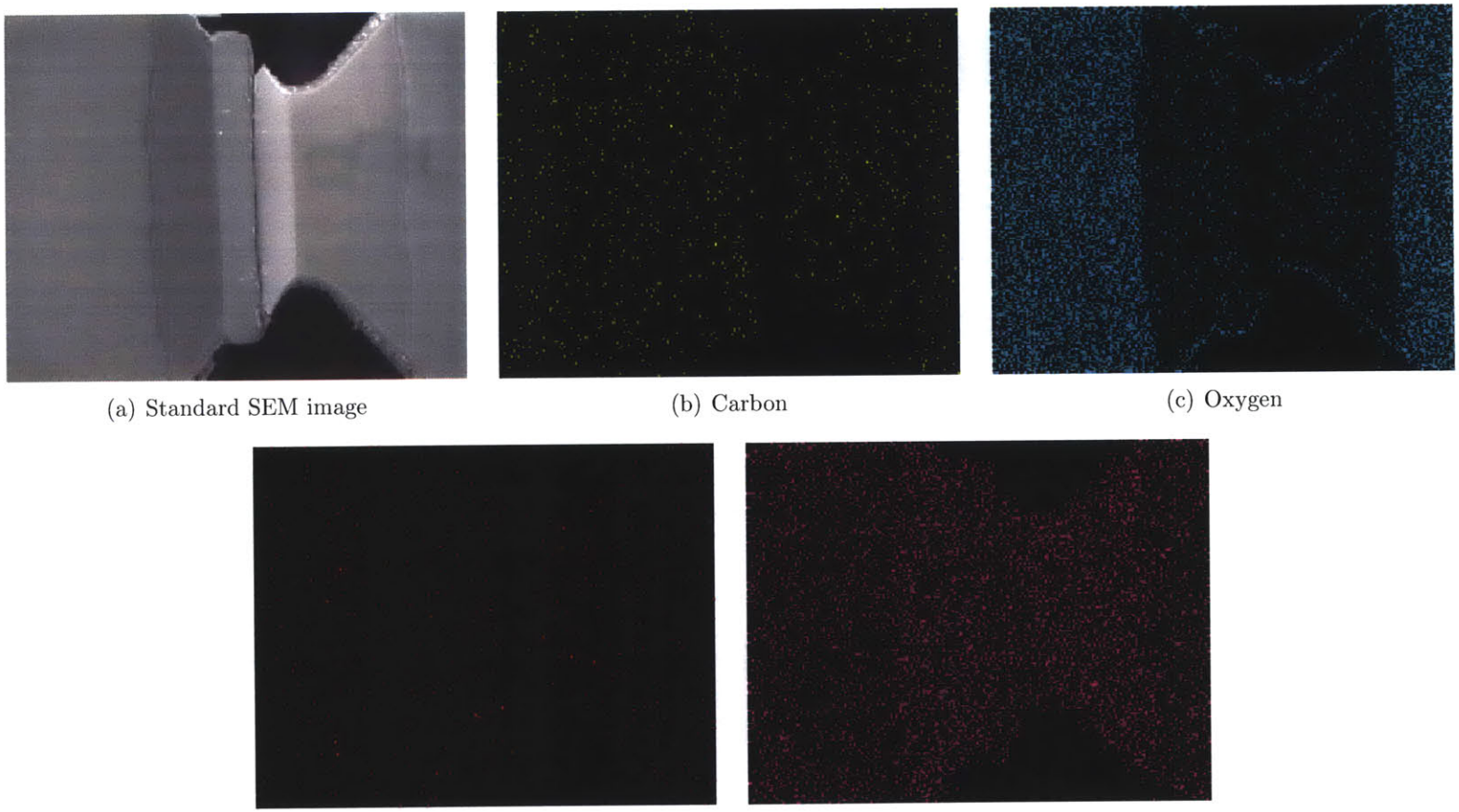
5.5.4 Re-Sharpening the Notch

With the notches definitively free of nitride as well as oxide, attempts were made to re-sharpen them with a short second dip in KOH. This was not attempted on the devices from the 1.0 version of the process because the notches of those devices are covered with oxide, which masks KOH.

Prior to the KOH dip, the devices were immersed in 50:1 H_2O:HF for 30 seconds to remove any native oxide and it was microscopically examined while underwater to confirm no bubbles were adhering to the surface, a potential micro-masking hazard. Pre- and post-fracture images of a specimen dipped in a 20% KOH solution at 80°C for 60 seconds are in Figure 5-29. The notch was not visibly altered by the etch, but the area surrounding the notch exhibits the faceting characteristic of KOH.

The specimen in Figure 5-29 is a typical result; none of the die re-etched for 60 seconds fractured well. Assuming the notches were sharpened by the dip, there being no reason to suppose otherwise, the specimen's failure to fracture well is most likely a consequence of notch shielding [6].

Notch shielding [107] occurs when the stress flow around a single notch is distorted



(a) Standard SEM image

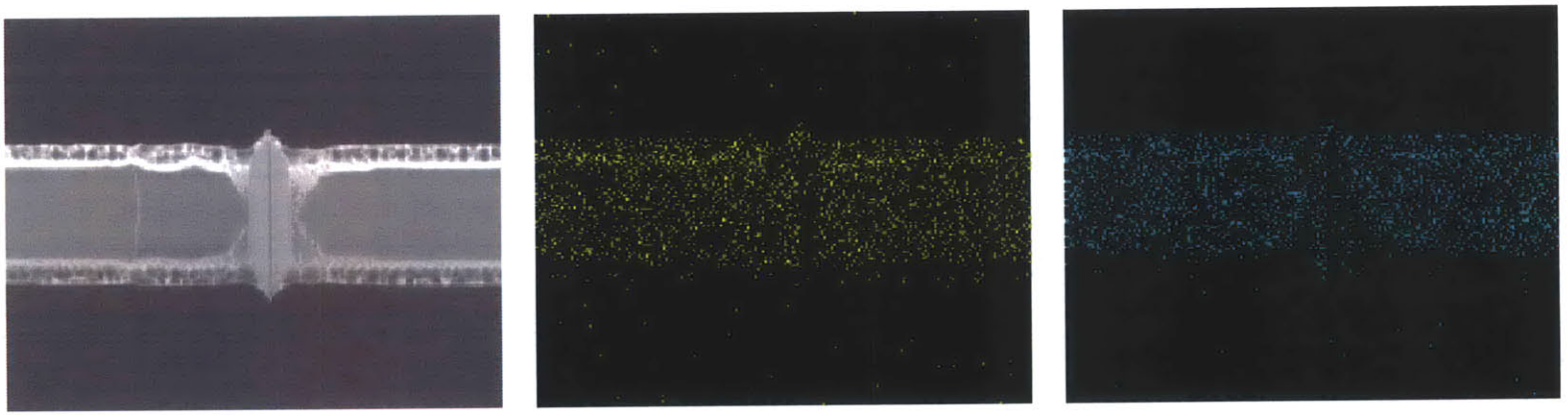
(b) Carbon

(c) Oxygen

(d) Nitrogen

(e) Silicon

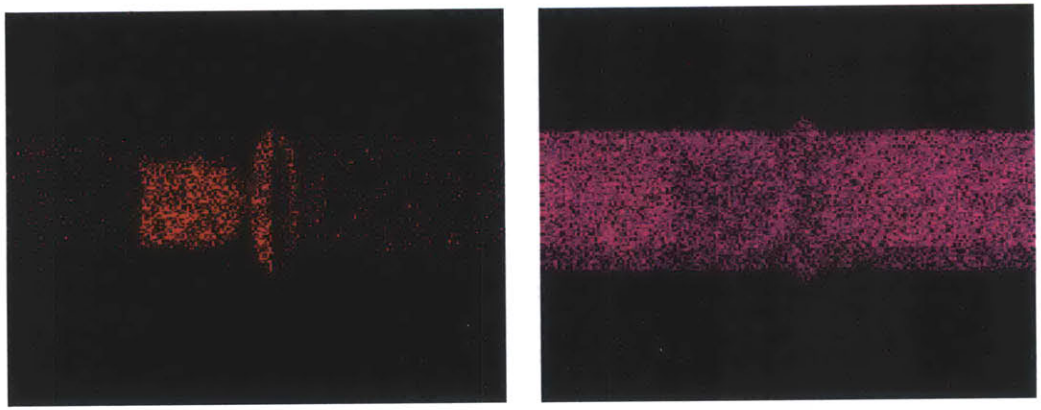
Figure 5-27: Element maps of die 51: oxidized, nitride-stripped, fractured. Note the uniformly distributed carbon and nitrogen traces (except on the right side of the trench, which was partially obscured from the detector), as well as the complementarity of the increased silicon signal in and around the trench with the increased oxide signal outside those areas.



(a) Standard SEM image

(b) Carbon

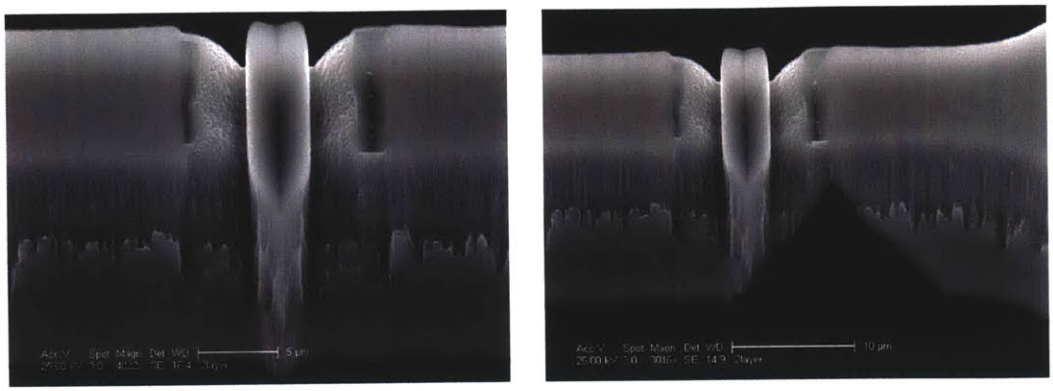
(c) Oxygen



(d) Nitrogen

(e) Silicon

Figure 5-28: Element maps of die 65: fractured. Note the strong nitrogen signal in and around the KOH trench, indicating those areas are covered with silicon nitride. The oxygen signal is uniform over the specimen because no thermal oxide has been grown.



(a) Before (b) After

Figure 5-29: SEM Images of the same KOH-sharpened second prototype specimen before and after fracture. Note the additional KOH etching visible in both images as well as the material ejecting fracture.

by the presence of other notches of similar size. This distortion can lead to an increase in the apparent toughness of a specimen. In this case, the increased fracture stress associated with the shielding leads to material ejection.

In an effort to re-sharpen the notch without creating shielding notches, a second set of die were etched with KOH for only 10 seconds. The fracture results (Figure 5-30) were indistinguishable from die that had not been re-sharpened (Figure 5-23); a wedge of material bound by (111) planes was ejected from the tip of the notch. It is unlikely notch-shielding played a role in the fracture of these dies, for the etch was too short to create the necessary secondary notches, and none are visible in Figure 5-30. The similarity of the fractures to those of specimens that have not been etched for a second time suggests the notch was not sufficiently re-sharpened if it was re-sharpened at all.

There may be a process window for re-sharpening where the notches can be effectively sharpened without creating shielding notches with an etch between 10 seconds and 60 seconds, but no more devices were available for testing. Regardless, the third version of the fabrication process (described in the next section) is considerably more robust than such a closely timed re-sharpening process is likely to have been, if it could have been made to work at all.

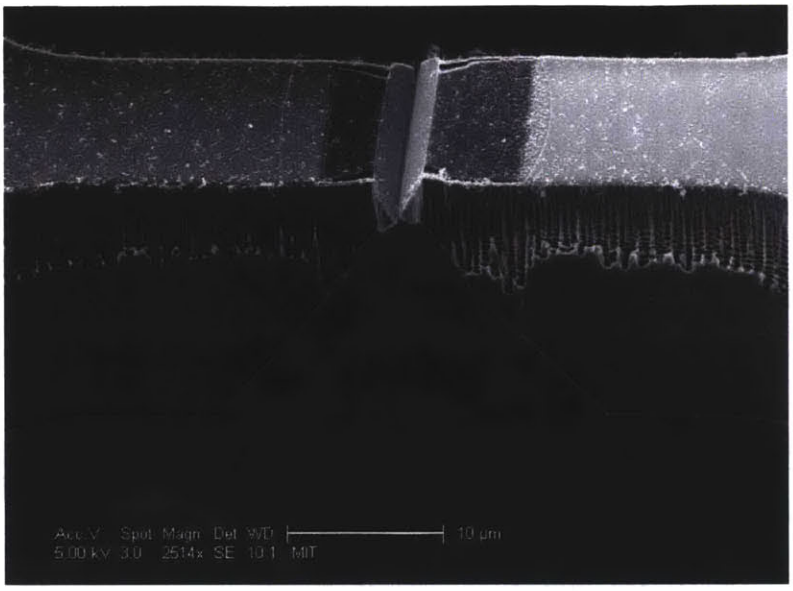


Figure 5-30: A SEM image of a specimen fractured after immersion in KOH for 10 seconds for re-sharpening. Note the absence of shielding notches, as well as the material ejecting fracture very similar to that of specimens that were not re-sharpened (Figure 5-23).

5.6 Fabrication Process 3.0

Version 3.0 of the fabrication process is conceived as a more elegant version of the re-sharpening process. Dipping finished die from the 2.0 version of the process into KOH is a poor solution because the entire notch area is exposed, and therefore etched, but it does establish that complex two and a half dimensional structures (i.e. all the device layer geometry including the zippers and flexures) can be masked with a conformal thermal oxide. Taking advantage of this masking discovery, the process is reversed.

In the reversed process, an initial nitride deposition and patterning defines areas that will become holes in the thermal oxide grown after the device layer DRIE defines the specimens, flexure structures, and actuators. A brief KOH etch is then done with the thermal oxide as a mask. The electrical contact areas are etched, but so is a small area of the specimen, leaving a full KOH notch. See Figure 5-31 for an overview of the process and Appendix A.5 for a complete description.

Unfortunately, all of the highly doped p-type wafers from SQI had been consumed, so the 3.0 version of the process is carried out on lightly doped wafers of unknown

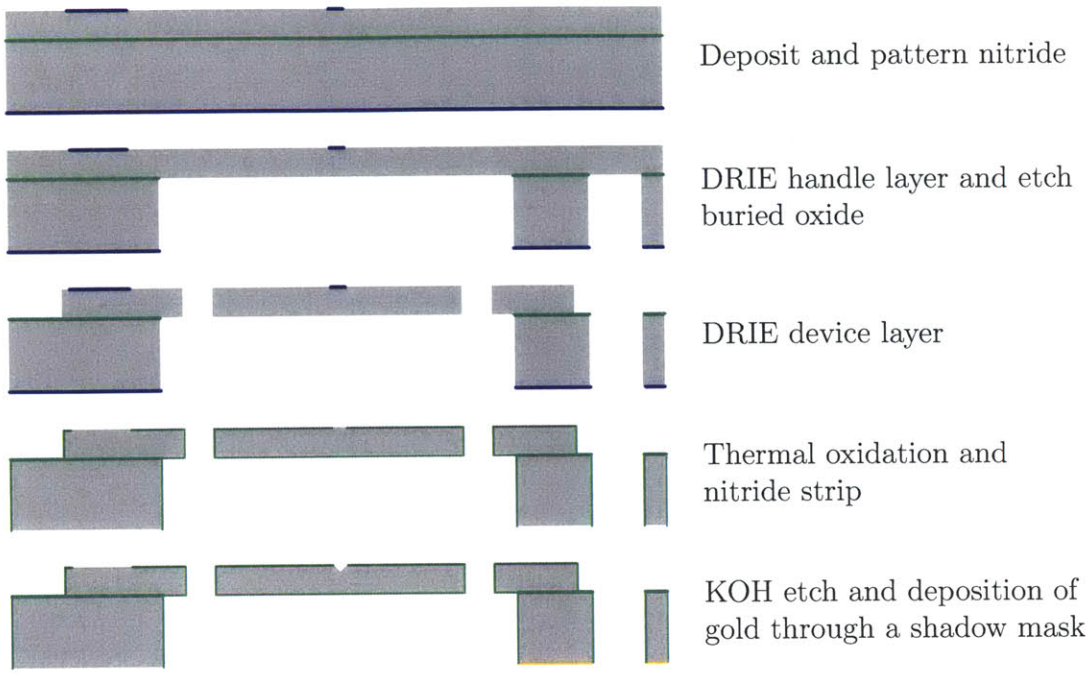


Figure 5-31: Variable capacitor fabrication process version 2.0. Note the KOH notch is covered with silicon nitride during the thermal oxidation.

type from an unknown vendor. The principal consequence of this is the formation of a Schottky diode at each of the wire bonds. Although the diodes can be broken-down to drive the actuator, they present a substantial obstacle at the low voltages employed for measuring capacitance.

The upside of the new wafers is that they are more or less pristine, so changes can be made to the handle layer etch mask. Based on experience gained during the first two fabrication runs, the size of the relief beneath the device layer structure, the gap around the die, and the epoxy holes are all shrunk. The new and old handle layer patterns are overlaid in Figure 5-32, where these changes can more easily been seen. The motivation for the changes is to make the etch more uniform, to improve support for the device layer structure, and to reduce the size of the device layer membranes.

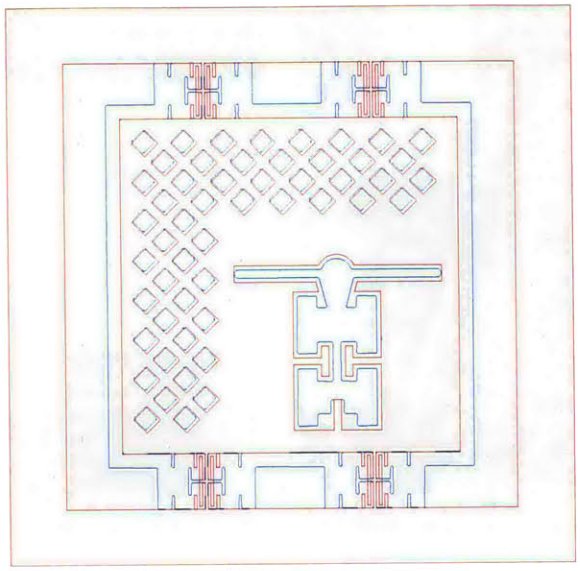
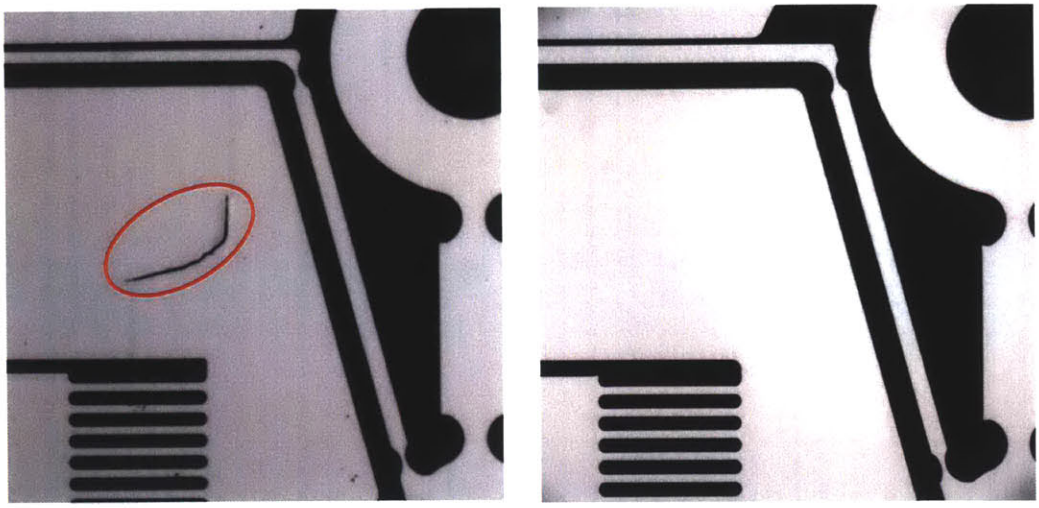


Figure 5-32: The new and old handle layer masks overlaid. The new version is in blue. Note the shrunken gap around the die, epoxy holes, and relief.

5.7 Testing the Third Prototype

The changes to the handle layer DRIE mask resulted in cleaner breakout tabs and the elimination of cracks in the device layer structure (Figure 5-33). The larger separation between the breakout tabs and their halos produced a more complete etch, leaving a thinner, better defined tab, that was both easier to break and easier to cut with the excimer laser. Cutting the tabs with a laser remained preferable because of the reduced risk of particulate contamination. The superior support of the smaller handle relief also eliminated the tendency of the device layer structure to crack during fabrication, a significant yield improvement.

Using the nitride as a diffusion barrier during oxidation, and then stripping the nitride to create a window in the thermal oxide produces a $3\,\mu$m tall rectangular feature the width of the specimen. Because the oxide deposition is conformal, the subsequent KOH etch does not "see" the sides of the specimen; there is no difference in the manner in which a normal rectangular feature on a pristine wafer would be etched and how the rectangular feature on the specimen is etched. A post-etch micrograph of the specimen (Figure 5-34) shows that the notch is somewhere between the full



(a) Cracked device layer structure (first version of mask)

(b) Un-cracked device layer structure (second version of mask)

Figure 5-33: Images of devices fabricated with the first and second versions of the handle layer DRIE mask.

(Figure 2-28(a)) and partial (Figure 2-28(b)) notches of Section 2.2.3.

Despite the notch not running fully across the specimen, the resulting fractures are of quite high quality (Figure 5-35). The specimens fracture without ejecting material and re-seal leaving only a 15-20 nm gap, despite the somewhat larger than nominal thickness (25 vs. 20 μm) and a certain amount of resist burn-through, which damaged the upper portion of the specimen. Etching the notch after all high temperature processing completely eliminates the blunting problems seen in versions 1.0 and 2.0 of the process.

Post-fracture, actuator function was confirmed by applying a potential, and observing the movement of the zipping cantilever. No arcing, or other ill-effects were observed up to 150 V. Though capacitance could not be measured on account of the Schottky diodes at the silicon-wire bond interface, the third version of the fabrication process did establish that high quality fracture surfaces can be integrated with a zipping electrostatic actuator.

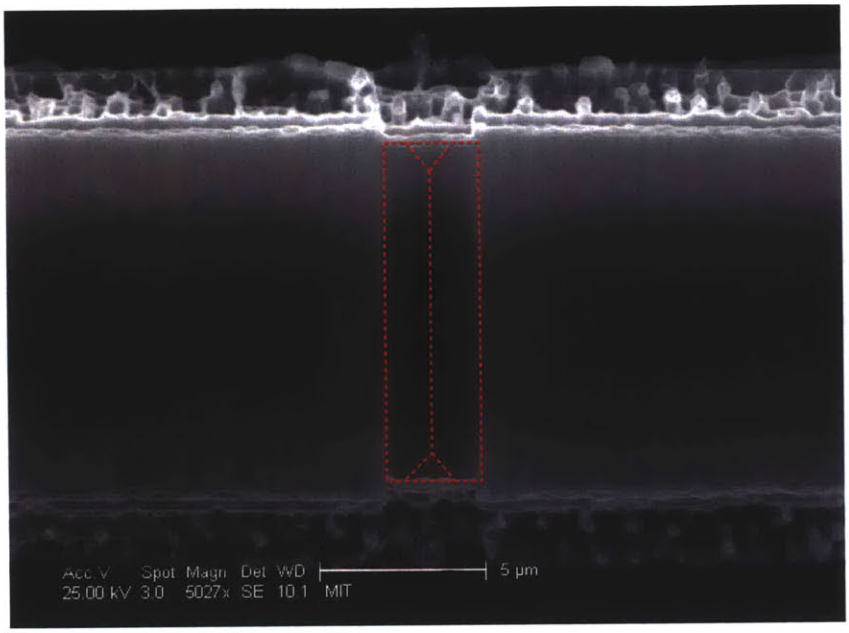


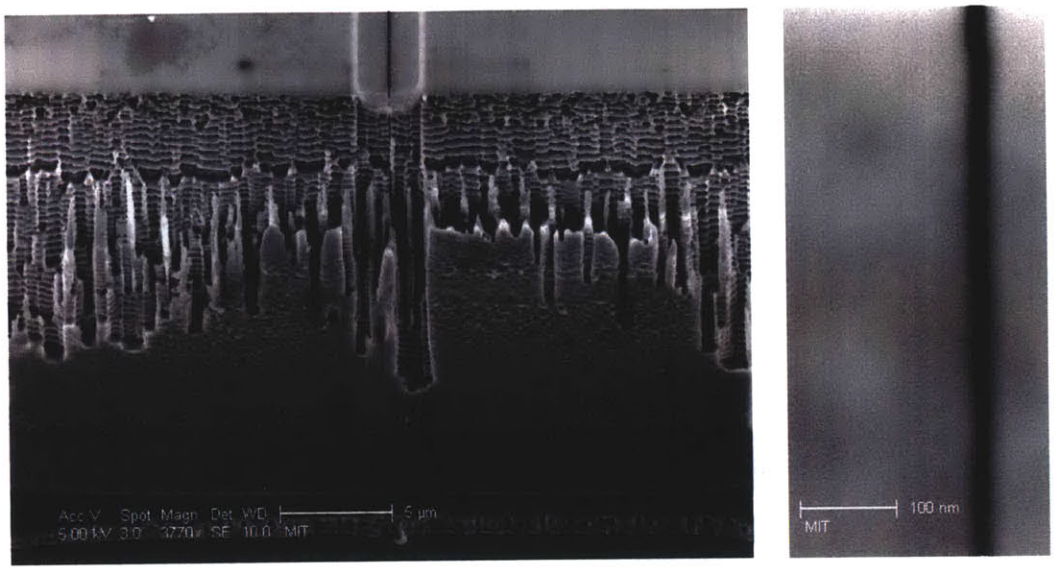
Figure 5-34: Because a rectangular region the width of the specimen is exposed to the KOH, version 3.0 of the fabrication process does not produce a full notch (Figure 2-28(a)), but rather a notch in between a full notch and a partial notch (Figure 2-28(b))

5.8 Packaging the Third Prototype

Packaging of the die from the third version of the fabrication process demonstrated the die can be eutectically assembled into the packages, but revealed a wire bonding problem. Electrical contact was made with the silicon, but to do so, the power setting on the wire bonding equipment had to be increased to the point that the die were damaged.

5.8.1 Eutectic Assembly

Die can be eutectically assembled into their packages without damaging the delicate device layer structure. The eutectic pre-form does flow (Figure 5-36) up the vertical surfaces of the handle layer, but not nearly far enough to pose a threat to the device layer structure. Contrary to instructions, the vendor deposited the preform in an L-shaped pattern aligned to the die-attach flow control holes, but such care is almost certainly not necessary. The thickness of the handle layer is great enough that the



(a) Side view of fractured specimen; fracture line is barely visible at this magnification.

(b) Line of fracture

Figure 5-35: Despite some resist burn though and thicker than nominal specimens (25 μm instead of 20 μm), specimens from the 3.0 version of the process fractured very well, with 15-20 nm gaps.

relief beneath the device layer structure provides sufficient protection.

Only one die was eutectically assembled because the vendor incorrectly believed the 400°C temperature of the eutectic process was damaging the bond pads. Subsequent die were assembled with the silver filled compound (JMI 7000) used with the die from the first version of the fabrication process. As will be discussed in the following section, those die also proved to be difficult to wire bond, so the eutectic assembly process is very likely not the cause of the problem. Nevertheless, future eutectic assembly should be done with a 300°C process; the lower temperature has been confirmed not to damage the stress concentrating notch by heating die on a hot-plate.

5.8.2 Wire Bonding Problems

As mentioned in the previous section, bonding wires to die from the third version of the fabrication process required more power than for the die from the first version of the fabrication process (die from the second version of the fabrication process were not

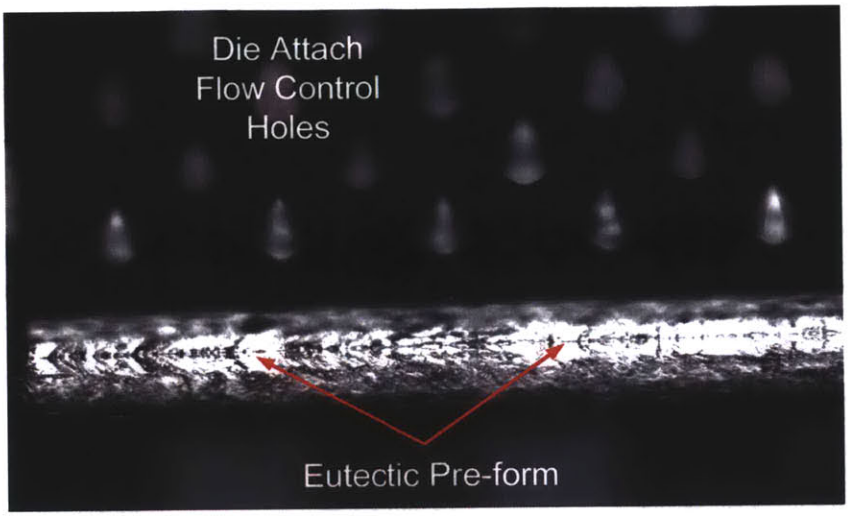
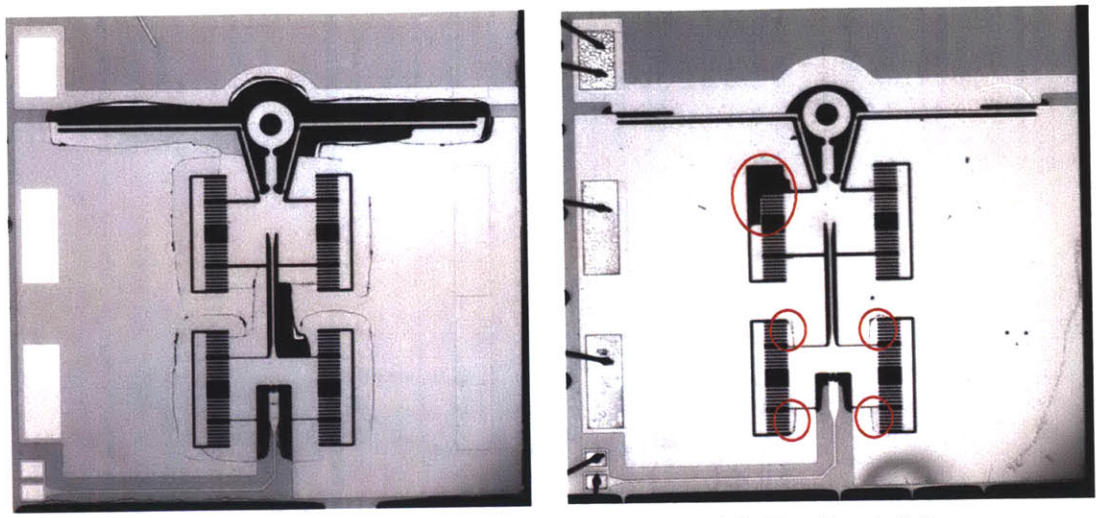


Figure 5-36: Micrograph of a eutectically assembled die. Portions of the image are out of focus because the side of the die is being viewed from an oblique angle. The eutectic pre-form has flowed up the sides of the die to a certain extent, but not nearly enough to pose a threat to the delicate device layer structure.

packaged). The application of higher power resulted in a dramatic yield reduction. Specimens were broken and chipped during bonding, and the device layer structure was damaged in a fashion reminiscent of die that had been placed in an ultrasonic bath (Figure 5-37). It was initially thought that the higher power was necessary because the bond pads had been damaged during the assembly process (see previous section), but even die assembled with JMI 7000 in the same fashion as the die from the first version of the fabrication process were difficult to bond. With that possibility eliminated, the two most likely causes of the problem are contamination and degradation of the silicon bond pads during KOH etching. The vendor's bonding equipment may also be at fault, but there is nothing specific to support this hypothesis.

Surface contamination may be the cause of the wire bonding difficulties. The final step in the first version of the fabrication process is the removal of the nitride covering the silicon bond pads, but final step of the third version of the fabrication process is to etch the dies with KOH. At the end of both processes, the devices are very fragile, and must be dried with care after any wet processing, e.g. KOH etching or nitride stripping with hot phosphoric acid. Due to equipment availability, wafers emerging from the hot phosphoric acid bath are rinsed with DI water and dried with a nitrogen



(a) Sonicated die

(b) Wire bonded die

Figure 5-37: Die damaged by sonication and wire bonding. Note the similar nature of the damage; the device layer structure is cracked near its support at the edge of the handle layer relief. The resemblance is less pronounced because the handle layer reliefs are different for the two die. See Figure 5-32, for a schematic illustration of the two different handle layer structure versions.

gun; wafers from the KOH bath are rinsed with DI water and then dipped in CMOS grade methanol, which is subsequently allowed to evaporate. It is possible a residue left behind by the methanol drying is responsible for the challenging wire bonds. If such contamination is the source of the problem, cleaning the wafers with piranha, drying them with a nitrogen gun, and then ashing for half an hour should correct the problem.

The more likely cause of the problem is roughening of the bond pad surface by the KOH etch. Wire bonding [52, 51] is "complex and not fully understood" [51], but given the "weld" between wire and pad is formed by the frictional heating of the interface, it is reasonable to assume surface finish plays a significant role. In the third version of the fabrication process, the bond pads are exposed during the etch to create the stress concentrating notches. Despite the brevity of the etch (5 minutes), the features are surprisingly well developed (Figure 5-38); the beginnings of a of an inverted pyramid are clearly visible in the SEM. The surface of the bond pad is no longer the polished wafer surface, but a surface produced by wet etching.

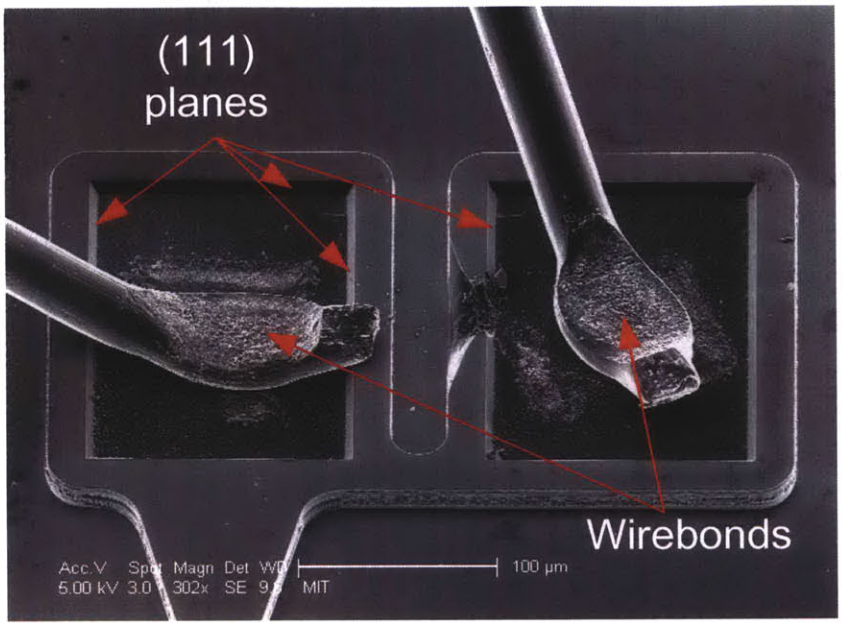


Figure 5-38: In version 3.0 of the fabrication process, the bond pads are exposed during the KOH etch to create the stress concentrating notches. Despite the brevity of the etch (5 minutes), the bond pads become KOH etch-pits, complete with (111) bounding planes.

The surface properties of the etched bond pads from version 3.0 of the process and the polished bond pads from version 1.0 of the process are in Table 5.2. The RMS surface roughness is calculated with the expression

$$R_q = \sqrt{\frac{1}{N}\sum_{i=1}^{N} z_i^2}, \tag{5.8}$$

where N is the number of points, and z_i is the height of the surface at each point. The skew, R_{sk}, of the surfaces is the "ratio of the third moment of the amplitude distribution and the standard deviation ... from the mean" [129] and is calculated with the expression

$$R_{sk} = \frac{1}{nR_q^3}\sum_{i=1}^{N} z_i^3. \tag{5.9}$$

In this context, a negative skew indicates the surface is composed primarily of valleys, while a positive skew corresponds to a surface composed primarily of peaks. Though both the RMS roughness and the skewness grow due to etching, the Peak to Valley measurement changes to most. This large change in the "peakiness" of the surface suggests there may be considerably less surface area over which the wire bond can form.

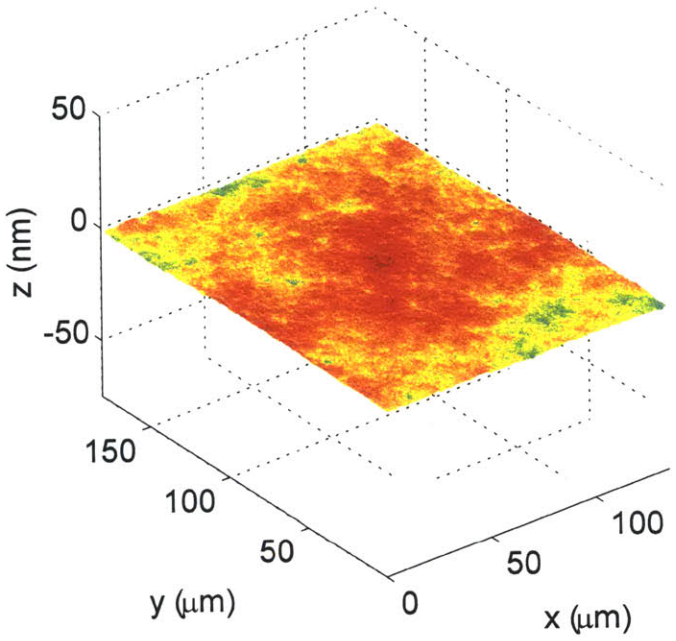
	Peak to Valley (nm)	**RMS Roughness, R_q (nm)**	**Skew, R_{sk}**
Version 1.0	7	≤ 1	-0.088
Version 3.0	306	9	-0.305

Table 5.2: Surface properties of bond pads from versions 1.0 and 3.0 of the variable capacitor fabrication process

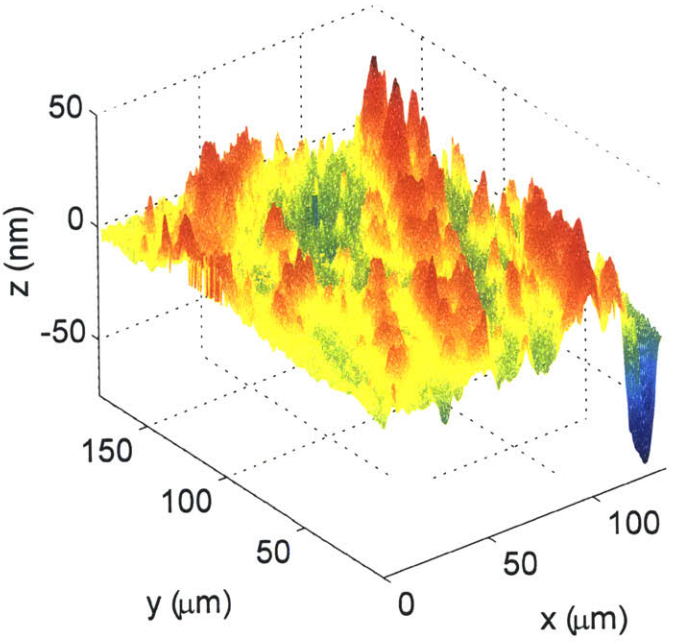
Viewing the topography itself makes the extent of the damage more clear. In Figure 5-39 are a pair of plots showing, at the same scale, the bond pad surfaces of the first and third prototypes; the third prototype pads that were difficult to bond, have a great deal more topography.

One could imagine the harsh topography of the third prototype pads improving bondability, since the higher friction coefficient of the rougher surface would produce more heat for a given amount of ultrasonic input, but the rougher surface also results in a smaller bond area, which in this case appears to dominate. A search of the literature revealed little to confirm or contradict this speculation, especially since wires are much more frequently bonded to metallized as opposed to bare silicon.

If removing any contamination with piranha and ashing fails to resolve the bonding problem, the pads could be metallized. A proper metallization would bring the wire bonding process within industry norms, perhaps even facilitating in house assembly. The metal could be deposited through a shadow mask, which has the advantage of being an established process, but the disadvantages of restricting the minimum bond pad size, which has consequences for the device' parasitics and of endangering the delicate device layer structure that would be in contact with the mask. A more elegant though much less well-established solution would be to deposit the metal film



(a) First Prototype



(b) Third Prototype

Figure 5-39: The surface topography of the bond pads on die from the first and third versions of the fabrication process, obtained with a NewView 5000 optical profilometer from Zygo Corporation of Middlefield, CT. The plots have the same scale. Note the substantial increase in surface roughness for the die from the third version of the fabrication process.

with an Offset Liquid Embossing (OLE) process similar to that of Wilhem, et. al. [146], followed by an annealing step. Bond pad metal deposited with OLE could be as small as desired and would pose no risk to the delicate device layer structure.

5.9 Summary

A process for the fabrication of variable capacitors with fracture surfaces as separable plates has been developed. A structure within the device layer of an SOI has been released without wet etching by relieving the supporting handle layer, and a zipping electrostatic actuator has been integrated with a pair of fracture surfaces. It has been determined that high temperature processing, though not thermal oxidation itself, blunts anisotropically etched structures such that fractures originating there eject material; sustained high temperatures are enough to cause this effect, even through a diffusion barrier. The packaging process requires more development, but with the integration of OLE for the deposition of metal, the last of the problems should be overcome.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

The introduction began with the question "Can fracture be useful?" As the prior art in Chapter 1 illustrated, the answer at the meso-scale is already "yes." The development in this thesis of a process for the fracture fabrication of pairs of matched complementary or nano-smooth surfaces, the design of a variable capacitor based on such fracture surfaces, and the execution of a fabrication process for such a capacitor makes the answer at the micro-scale "yes" as well.

A process and a specialized moment attenuating compliant mechanism were developed for the fracture fabrication of nano-smooth and complementary surfaces. The effects of specimen orientation, notch type, surrounding structure, and specimen thickness on fracture surface properties (roughness, planarity, etc.) were studied. In the absence of material ejection, complementary surfaces that re-sealed leaving only 15-20 nm gaps were relatively easy to produce. Nano-smooth surfaces were produced from (110) oriented 10 μm square specimens fully notched by anisotropic etching (KOH).

A variable capacitor employing fracture surfaces as its separable plates was designed. The system was optimized to minimize the stable surface separation by reducing the displacement at which the force between the capacitor plates dominates the spring force of the compliant mechanism; the zipping electrostatic actuator that

controls the surfaces' separation is stable when working against the spring force, but not the capacitive force.

Prototype variable capacitors with integrated actuators were fabricated. The process was evolved to eliminate the blunting effects of high temperature processing on the anisotropically etched notches. Such blunting resulted in material ejecting fractures unsuitable for use in a variable capacitor. By using the actuator's thermal oxide as an etch mask, the anisotropic etch to define the stress concentrating notches was moved to the end of the process, after all high-temperature processing is complete.

As the tortuous development of the capacitor fabrication process indicates, there are many subtle challenges to integrating fracture surfaces within a working MEMS device. Because of those challenges and limitations, further development of fracture based devices should be undertaken after a more thorough examination of the potential of anisotropically etched surfaces (Section 3.2).

6.2 Future Work

Three different avenues for future work are presented in the following section. Continuing in the same vein as this thesis, further work could be done to develop MEMS devices with embedded fracture surfaces. Alternatively, the trouble with high temperature process of the stress concentrating notches in Chapter 5 could be turned on its head, and a study made of the potential for toughening anisotropically etched structures. Striking off in a new direction, the potential of MEMS devices based on pairs of anisotropically etched surface could be more thoroughly explored.

6.2.1 Further Fracture Device Development

The most pressing piece of future work along the line of further developing fracture based devices is the execution of the 3.0 version of the variable capacitor process (Section 5.6) on properly doped wafers. The packaging difficulties discussed in Section 5.8 are anticipated to be a minor problem, and should be resolved with better wafer cleaning or metallization. If the resulting devices perform as outlined in Chap-

ter 4, the path will be cleared toward the development of micro-valves, dielectric spectroscopy instruments, and perhaps devices for the measurement of the Casimir Force, as outlined in Chapter 1.

The principal obstacle to employment of the variable capacitor device as an RF MEMS circuit element is its large parasitic capacitance, and the ensuing sub-par tuning ratio (Table 1.1). This problem may be overcome by fabricating the device layer structure atop a glass substrate similar to the processes described in [58] and [126]. Such a course would likely be a substantial undertaking, however, given the difficulties encountered developing the existing process.

The variable capacitor might benefit from other, more prosaic, modifications as well, such as the integration of a capacitive displacement sensor and the re-location of the zipper actuator. Integrating a metrology capacitor independent of the fracture surface electrodes would facilitate closed-loop control of their separation. Connecting the zipper directly to the specimen stage of the structure may have performance benefits (though at the potential cost of making the imperfections of the zipper more apparent at the fracture surfaces).

Several changes would also be advisable if the device were to enter volume production. Given that cost scales strongly with die-size, a re-design of the structure with an emphasis on reducing its extent would be well-considered. At the same time, the geometry of the handle layer relief could be re-worked to enable the relief to be etched with an anisotropic etch. Elimination of the long, DRIE etch of the handle layer would considerably reduce the expense of the process. Also, as discussed in Chapter 5, yield could be greatly enhanced by revising the masking for the device layer DRIE so that resist does not have to be deposited after the handle layer DRIE.

On the research end of the spectrum, it would be interesting to return to the fracture development devices of Chapter 2, perhaps with a handle layer relief to facilitate a dry release, and to make a thorough study of the effects of fracture specimen width, the possibilities for multiple parallel fracture specimens (Figure 4-26(c)), and of fracture specimens oriented with the (111) planes. The variable capacitor devices included specimens of varying widths as well as parallel specimens, both of which

performed well, but the two-stage process development device is more suited to fully exploring their potential, largely because it can be latched open for SEM examination of the surfaces. The production of larger areas without compromising surface finish (as increasing specimen thickness does) would be a significant accomplishment. Since smooth (111) planes were often the result of FIB notching and less than full anisotropically etched notching, it would also be intriguing the investigate specimens aligned with the (111) plane, which with (110) is a traditional silicon cleavage plane.

6.2.2 Toughening of Anisotropically Etched Structure

The conclusion from Chapter 5, that processing anisotropically etched notches at high temperature results in material ejecting fractures could, by reciprocity, be converted from a problem to a solution. As mentioned in the fracture process development chapter (Chapter 2), material ejection is characteristic of a high stress fracture. High temperature processing may therefore be a route to toughening anisotropically etched structures. Such structures are common in commercial MEMS devices, so a microfabricaiton compatible method for toughening them could be very attractive. To investigate the degree of toughening, two-stage devices (Section 2.2) dry-released with a handle layer relief, and then exposed to high temperatures could be fractured with the Flextester [116]. With the underlying handle layer material removed, friction between the probe tip and the substrate cannot contaminate the measurement. By fracturing a series of devices exposed to varying temperatures for varying times, the amount of toughening could be quantified and an optimized process developed.

The change in fracture behavior after high temperature processing of the anisotropically etched stress-concentrating notches is believed to be a consequence of diffusional smoothing; silicon atoms at the root of the notch diffuse to blunt the corner. Direct confirmation of this hypothesis could come from directly measuring the sharpness of the trench before and after high temperature processing. Though the sharpness of anisotropically etched notches has been measured by AFM [50], it is likely such experiments are really just measuring the diameter of the AFM tip. A better approach would be to image the notch with a TEM (similar experiments are described in [104],

but changes to the notch tip were not the emphasis of the study). The principal challenge of such a TEM study is likely to be the preparation of high quality thin specimens.

6.2.3 Anistotropically Etched Devices

Striking out in a new direction, a device incorporating parallel anisotropically etched surfaces along the lines of the one in Section 3.2 could be developed. Compared to the fracture based devices described in this thesis, such a device would have the advantages of larger surfaces, a smaller footprint, and a more compliant flexure. The flexure may be more compliant because the device is normally-open. When the surfaces are close to each other, the flexure bearing is near its maximum stroke, and can therefore dominate the forces of electrostatic pull-in without being particularly stiff. The reduced footprint of the device (due to the removal of the moment attenuating portion of the structure) is important because it is a potential antidote to the concept's principal weakness: the requirement for a very high quality bearing. The bearing must facilitate the approach of the surfaces without harming their parallelism. A smaller structure will feel the effects of wafer bow and residual stress less strongly than a larger one would; Abbe errors have less of an amplification factor.

Fortuitously, the SOI wafers for developing anisotropically etched devices are the same wafers that would be useful exploring fracture based devices oriented with the (111) plane. Two different objectives may be pursued with the same hardware.

Appendix A

Fabrication Processes

The fabrication processes discussed in the main body of the text are included here in full. The notes at the end of each process indicate the date it was approved the MIT's Microsystems Technology Laboratory (MTL) Process Technology Committee (PTC) and any modifications that have since been made to the process. Also included are some sub-processes alluded to in the main processes, such as depositing a double thickness of resist or mounting a wafer on a handle.

A.1 Single Stage Device Fabrication Process

Mentioned in Section 2.1, this is the process for fabricating the single stage fracture process development device. In the process, the device layer of an SOI wafer is etched with DRIE, and then the structure is released by wet-etching the underlying oxide. To prevent stiction, the release etch is arrested by diluting the HF with water so that the device is never exposed to air.

Single Stage Device Fabrication Process

June 15, 2002

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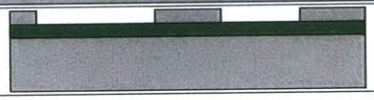
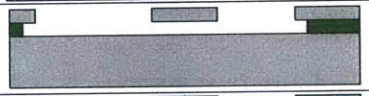
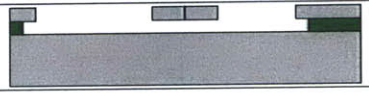
	Meta Description	Description	Lab	Machine	Recipe	Diagram
1	Preparation	Blank 300 mm SOI wafer, 10 μm device layer, 300 μm handle				
2	DRIE device layer to create specimen	HMDS	TRL	HMDS	25 Å	
3		Deposit Photoresist	TRL	Coater	AZ 4620	
4		Pre Bake	TRL	Pre-Bake Oven	90° C, 60 minutes	
5		Exposure	TRL	EV-1		
6		Develop	TRL	Photo Wet	2 minutes	
7		Post Bake	TRL	Pre-Bake Oven	90° C, 30 minutes	
8		DRIE	TRL	STS-n	Through device layer ~ 8 minutes MIT 59A	
9		Strip Photoresist	TRL	Acid Hood 2	Piranha, 10 minutes	
10	Separate the Dies	Die Saw	ICL	Die Saw	220 microns of die separation	
	GOLD CONTAMINATED					
11	Affix dies to the bottom of a Petri dish with Crystal Bond					
12	Etch oxide layer to release flexure and specimen	HF Etch	EML	Acid Hood	HF release, 45 minutes, arrest etch by dilution	
13	Fracture the specimen	Fracture		Probe Station	Carefully	

A.2 Two Stage Device Fabrication Process

From Section 2.2, this is the process for fabricating the two-stage fracture process development device. The principal alteration from the process for the single stage device fabrication process (Appendix A.1) is the addition of a KOH etch to define the stress concentrating notches. Other additions, such as the deposition and patterning of a thermal oxide, support the KOH etch.

Two Stage Device Fabrication Process

Oct 21, 2002

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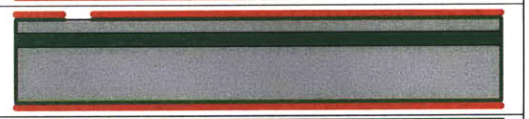
	Meta Description	Description	Lab	Machine	Recipe	Diagram
1	Preparation	Blank 100 mm SOI wafer, 10 μm device layer, 300 μm handle				
2	KOH Etch to find crystal planes and create stress concentration notches	RCA	ICL	RCA	RCA	
3		Grow 150 nm oxide	ICL	Tube5D	Wet or Dry	
4		HMDS	TRL	HMDS	25 Å	
5		Deposit Photoresist	TRL	Coater	OCG 825	
6		Pre Bake	TRL	Prebake	30 min at 90C	
7		Exposure	TRL	EV1	2 seconds	
8		Develop	TRL	Photo Wet	~2 minutes	
9		Post Bake	TRL	Postbake	30 min at 120 C	
10		Oxide Etch (BOE)	TRL	Acid Hood 2	BOE (~90 seconds)	
11		Strip Photoresist	TRL	Acid Hood 2	Piranha	
12		KOH	ICL	TMAH-KOH	25wt% for 2 min	
13		Post KOH Clean	TRL	Acid Hood 1	Yellow Piranha, 10 minutes	
14			TRL	Acid Hood 1	Green Piranha, 10 minutes	
15			TRL	Acid Hood 1	50:1 HF Dip, 15sec	
16		Strip Oxide	TRL	Acid Hood 1	BOE, 2 min	
17	DRIE device layer to create specimen	HMDS	TRL	HMDS	25 Å	
18		Deposit Photoresist	TRL	Coater	OCG 825	

19		Pre Bake	TRL	Pre-Bake Oven	30 min at 90C	
20		Exposure	TRL	EV-1	2 seconds	
21		Develop	TRL	Photo Wet	~2 minutes	
22		Post Bake	TRL	Pre-Bake Oven	30 min at 120 C	
23		DRIE	TRL	STS-2	MIT69, ~15 min, watch	
24		Strip Photoresist	TRL	Acid Hood 2	Piranha, 10 minutes	
25	Separate the Dies	Die Saw	ICL	Die Saw	220 microns of die separation	
			GOLD CONTAMINATED			
26	Affix dies to the bottom of a Petri dish with Crystal Bond					
27	Etch oxide layer to release flexure and specimen		EML	Acid Hood	HF release, 45 minutes, dilution arrested	

Change Log

October 21, 2002	Process Created
November 18, 2002	Process Approved, wafer diameter corrected (previously listed as 300 mm), KOH step changed to be done at KOH-TMAH hood physically located in EML, but administratively in ICL. The KOH hood in the diesaw room is gold contaminated.

A.3 Variable Capacitor Fabrication Process 1.0

From Section 5.1, this is the 1.0 version of the process for fabricating the variable capacitor device. Based on an accelerometer process [1], a nitride layer is deposited and patterned as a KOH mask, the device layer of the SOI is KOH etched to create stress concentrating notches, the nitride is patterned a second time for use a diffusion barrier, the handle layer of the SOI is DRIE'd to create a relief, the device layer is etched to define the primary structure, a thermal oxide is deposited as a dielectric for the actuator, and the contacts are exposed with a hot phosphoric etch.

Variable Capacitor Fabrication Process 1.0

This process is designed to produce device layer variable capacitors that are released within the STS

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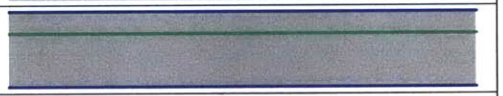
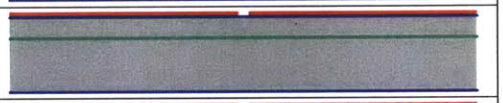
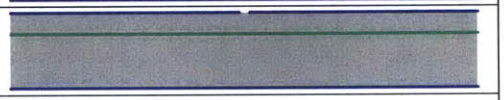
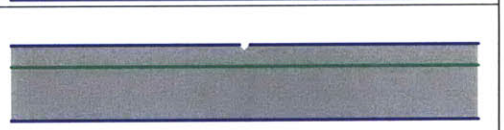
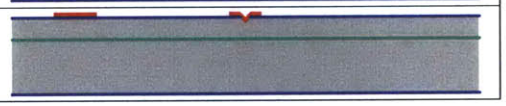
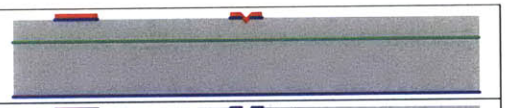
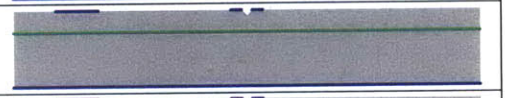
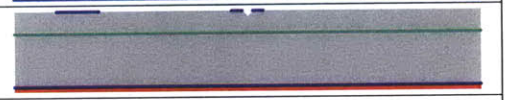
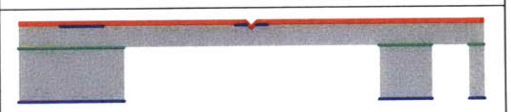
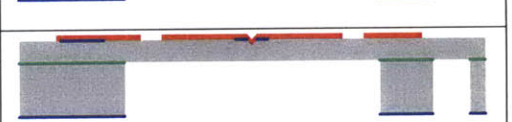
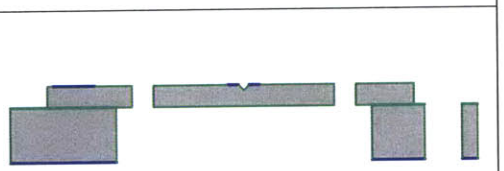
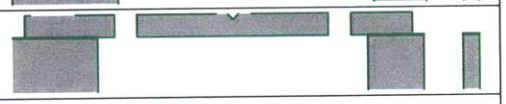
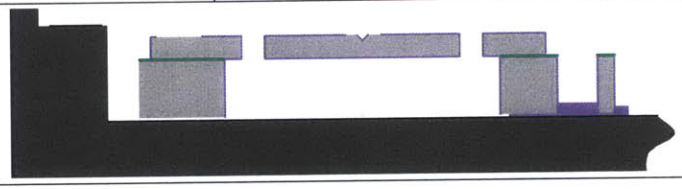
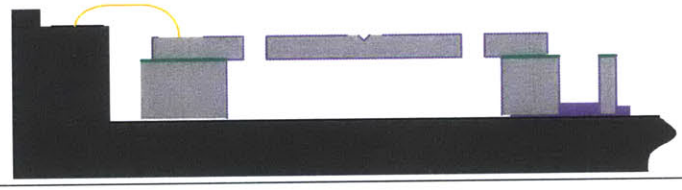
	Meta Description	Description	Lab	Machine	Recipe	
1	Wafers	Virgin 100 mm DSP SOI wafer, 10-20 μm device layer, 300 μm handle				
2	Deposit Nitride	RCA	ICL	RCA		
3		LPCVD Nitride		6D-nitride	150 nm	
4	Pattern Nitride I	HMDS	TRL	HMDS		
5		Deposit PR		coater	OCG-825	
6		Prebake		prebakeovn	30 minutes, 90°C	
7		Expose		EV-1	2 seconds	
8		Develop		photo-wet	OCG 934 1:1 1 min	
9		Postbake		postbake	30 minutes, 120°C	
10		Etch Nitride		AME5000	Chamber A: NITRIDE CF4, 66 seconds for 150 nm	
11		Strip Photoresist		acidhood2	piranha	
12	KOH Etch and Clean	KOH Etch	ICL	TMAH-KOHhood	5 minutes	
13		Yellow Piranha	TRL	Acidhood	Yellow, 10 min	
14		Green Piranha		Acidhood	Green, 10 min	
15		HF Dip		Acidhood	50:1, 15 seconds	
16	Pattern Nitride II	HMDS	TRL	HMDS		
17		Deposit PR		coater	OCG-825	
18		Prebake		prebakeovn	30 minutes, 90°C	
19		Expose		EV-1	2 seconds	
20		Develop		photo-wet	OCG 934 1:1 1 min	
21		Postbake		postbake	30 minutes, 120°C	

22		Nitride Etch		AME5000	Chamber A: NITRIDE CH4, 66 seconds for 150 nm	
23		Strip Photoresist		Acidhood2	piranha	
24	Handle Layer Etch	HMDS	TRL	HMDS		
25		Deposit PR		coater	AZ-4620	
26		Prebake		prebakeovn	60 minutes, 90°C	
27		Expose		EV-1	22 seconds	
28		Develop		photo-wet	AZ-440, 2 min	
29		Postbake		postbake	30 minutes, 90°C	
30		Etch Handle Layer		STS-1	NITRIDE for 4-5 min then MIT59	
31		Etch Buried Oxide		acidhood2	BOE, 15 minutes	
32		Strip Photoresist		acidhood2	piranha	
33	Device Layer Etch	HMDS	TRL	HMDS		
34		Deposit PR		coater	OCG-825 double coat	
35		Prebake		prebakeovn	30 minutes, 90°C	
36		Expose		EV-1	6 seconds	
37		Develop		photo-wet	OCG 934 1:1	
38		Postbake		postbake	30 minutes, 120°C	
39		Etch Device Layer		STS-1	STShall, wafer mounted on handle	
40		Strip Photoresist		acidhood2	piranha	

41	Grow Oxide	RCA	TRL	rca-TRL	blow dry with air gun and then put empty cassette in the SRD	
42		Grow Oxide		A2-WetOxBond	300 nm of oxide, Recipe #5, 45 minutes of wet oxidation	
43	Expose Contacts	Remove Oxy-Nitride		acidhood2	BOE:DI Water 1:1 for 70 seconds, 65 nm/min – remove 750 A of oxide	
44		Strip Nitride	ICL	nitrEtch-HotPhos	35 minutes, 4.5 nm/minute	
45	Separate Dies	Break tabs with wafer mounted on porous aluminum vacuum chuck				
46	Package	Epoxy the die into a ceramic package with high temperature epoxy. Die has features to prevent the epoxy from flowing up and damaging device layer structure.				
47	Wiring into Package	Direct from package pads to silicon	ICL	Goldwire, 330°C, ball size 12		

Notes:

1. Structure has been modeled to confirm that device layer can withstand pressure forces when on coater vacuum chuck
2. High temperature epoxy: Cotronics Corporation (www.cotronics.com), Duralco 124, good to 650°F (340°C)
3. Wirebonding directly to silicon has been tested
4. Practice handle layer DRIE etch on a scrap SOI wafer.
5. Alignment targets will be unusually wide because the 2nd Nitride mask and the handle layer DRIE mask will be made from transparencies.
6. It is probably possible to use the STS' selectivity for nitride over oxide to strip the nitride with DRIE rather than hot phosphoric acid, but I think it's more conservative to use the hot phosphoric. Poor uniformity of the STS could cause significant etching of the underlying silicon.
7. Package is Kyocera PN: KD-78382-G-1 (or equivalent from NTK). Lid is HRC-372-21-50MT/100-GK. Sealing is done by Golden Altos, Inc. of Milpitas, CA.

Change Log

February 13, 2004	Process Created
March 12, 2004	Process Approved
April 21, 2004	Nitride etches changed from STS to AME5000
June 23, 2004	Added oxy-nitride etch before stripping nitride in hot phosphoric acid.
December 3, 2004	Note added to AME5000 process steps indicating that etching will be done in chamber A
April 28, 2005	Double coating with OCG 825 for device layer etch

A.4 Variable Capacitor Fabrication Process 2.0

The 2.0 version of this process (from Section 5.4) differs from the 1.0 version principally in the addition of nitride deposition and patterning steps after the KOH notch etching step. The notches are thus covered with a nitride diffusion barrier during oxidation, preventing any oxidation blunting.

Variable Capacitor Fabrication Process 2.0

This process is designed to produce variable capacitors from virgin SOI's

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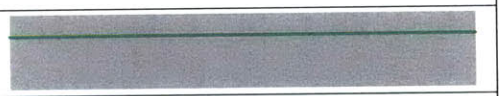
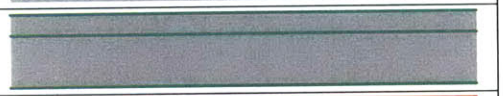
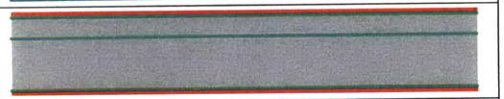
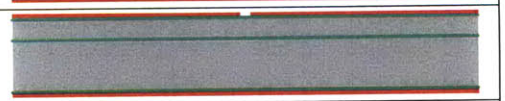
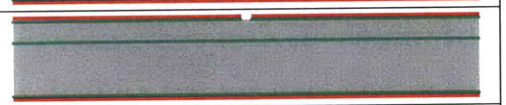
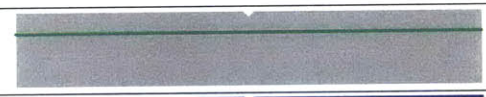
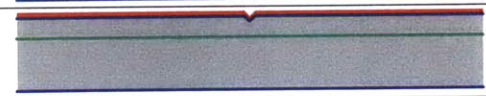
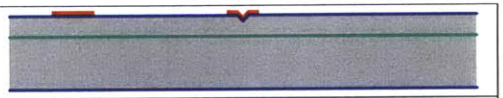
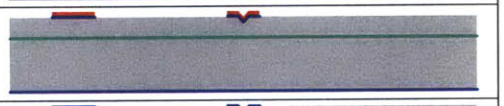
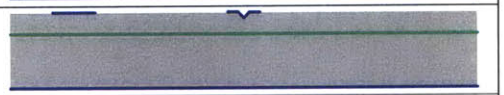
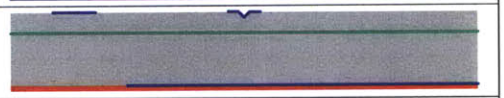
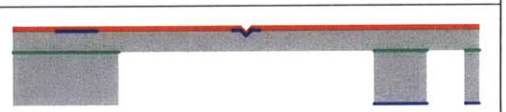
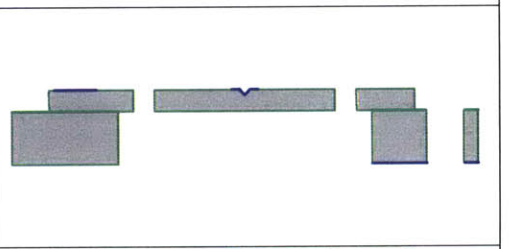
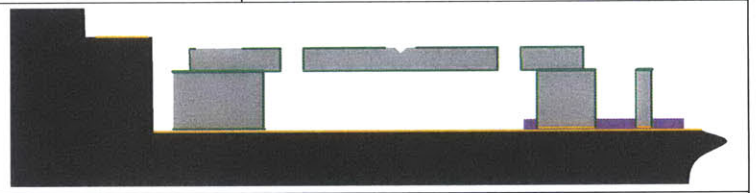
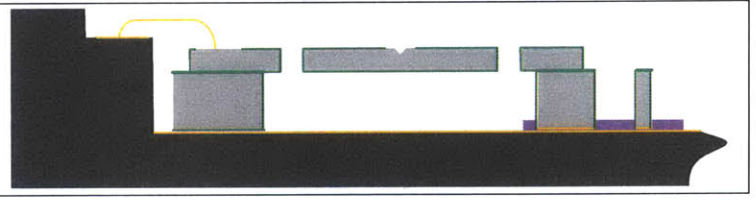
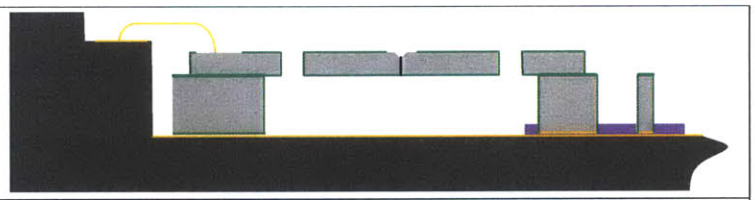
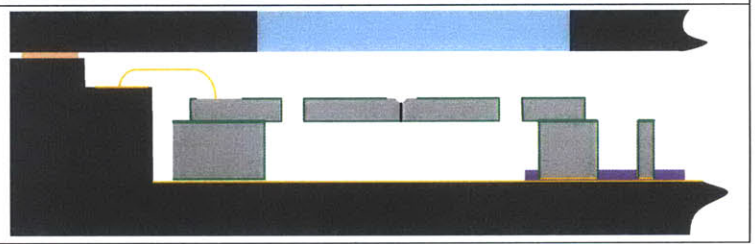
	Meta Description	Description	Lab	Machine	Recipe	
1	Wafers	Virgin 100 mm DSP SOI wafer, 10-20 μm device layer, 300 μm handle				
2	Thermal Oxidation	RCA	ICL	RCA		
3		Oxidation		Tube5D	1 um	
4	Pattern Device Side Oxide	HMDS	TRL	HMDS		
5		Deposit PR		coater	OCG-825	
6		Prebake		prebakeovn	30 minutes, 90°C	
7		Expose		EV-1	2 seconds	
8		Develop		photo-wet	OCG 934 1:1 1 min	
9		Postbake		postbake	30 minutes, 120°C	
10		Etch Oxide		acidhood2	BOE, 90 seconds	
11		Strip Photoresist		acidhood2	piranha	
12	KOH Etch and Clean	KOH Etch	ICL	TMAH-KOHhood	20 minutes	
13		Yellow Piranha	TRL	Acidhood	Yellow, 10 min	
14		Green Piranha		Acidhood	Green, 10 min	
15		HF Dip		Acidhood	50:1, 15 seconds	
16	Strip Oxide			Acidhood	BOE, 2 minutes	
17	Deposit Nitride	Low Stress Nitride	ICL	VTR	150 nm	
18	Pattern Device Side Nitride	HMDS	TRL	HMDS		
19		Deposit PR		coater	OCG-825	
20		Prebake		prebakeovn	30 minutes, 90°C	
21		Expose		EV-1	2 seconds	

22		Develop		photo-wet	OCG 934 1:1 1 min	
23		Postbake		postbake	30 minutes, 120°C	
24		Etch Nitride	ICL	AME5000	Chamber A: NITRIDE CF4, 66 seconds for 150 nm	
25		Strip Photoresist	TRL	acidhood2	piranha	
26	Pattern Handle Layer	HMDS	TRL	HMDS		
27		Deposit PR		coater	AZ-4620	
28		Prebake		prebakeovn	60 minutes, 90°C	
29		Expose		EV-1	22 seconds	
30		Develop		photo-wet	AZ-440, 2 min	
31		Postbake		postbake	30 minutes, 90°C	
32		Etch Handle Layer		STS-2	NITRIDE for 4-5 min then MIT59	
33		Etch Buried Oxide		acidhood2	BOE, 15 minutes	
34		Strop Photoresist		acidhood2	piranha	
35	Device Layer Etch	HMDS	TRL	HMDS		
36		Deposit PR		coater	OCG 825 (double coat)	
37		Prebake		prebakeovn	60 minutes, 90°C	
38		Expose		EV-1	6 seconds	
39		Develop		photo-wet	OCG 934 1:1 1 min	
40		Postbake		postbake	30 minutes, 90°C	
41		Etch Device Layer		STS-2	STShall, wafer mounted on handle	
42		Strip Photoresist		acidhood2	piranha	

43	Thermal Oxidation	RCA	TRL	rca-TRL	blow dry with air gun and then put empty cassette in the SRD	
44		Grow Oxide		A2-WetOxBond	300 nm of oxide, Recipe #5, 45 minutes of wet oxidation	
45	Expose Contacts	Remove Oxy-Nitride	TRL	acidhood2	BOE:DI Water 1:1 for 70 seconds, 65 nm/min – remove 750 A of oxide	
46		Strip Nitride	ICL	nitrEtch-HotPhos	35 minutes, 4.5 nm/minute	
47	Handle Layer Contacts	Deposit gold	TRL	e-beam	20 nm of titanium, 300 nm of gold, deposited through a shadow mask	
48	Dice Wafer	Break tabs with wafer mounted on porous aluminum vacuum chuck or cut the tabs by laser machining				
49	Assemble	Package is Kyocera PN: KD-78382-G-1 or NTK IDK24F1-167MAL. Adhesive is JMI 7000. Golden Altos of Milpitas CA does assembly, wirebonding, and sealing.				
50	Wirebond	Aluminum or gold wire, see wiring diagram (8 bonds)				

51	Fracture	Done with external probe, followed by examination in SEM to check fracture surfaces.	
52	Seal	HRC-372-21-50MT/100 GKL, Mil-Std-883, Method 1018 or Mil-Std-883, Method 5005, Table IV, Group D6 test	

Notes:

1. Double coating with OCG 825 has been tested with 3 um features.

Change Log

March 1, 2005	Process created by modifying Variable Capacitor Fabrication Process 1.0.
March 7, 2005	Process approved by PTC
April 28, 2005	Patterning of handle side nitride removed

A.5 Variable Capacitor Fabrication Process 2.0 (Rework)

The 2.0 (Rework) process (from Section 5.4) is the practical cousin of the 2.0 process. The only wafers available for processing had already been through the 1.0 version of the process up though the handle DRIE and buried oxide etch steps. This process was conceived as a variant of the 2.0 process that could be applied to these non-virgin wafers.

Variable Capacitor Fabrication Process 2.0 (Rework)

This process is designed to rework partially fabricated device layer variable capacitors

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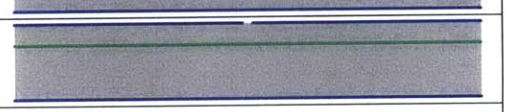
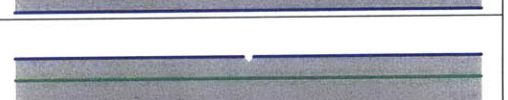
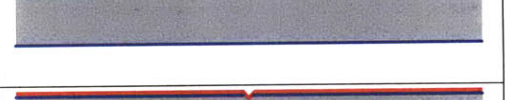
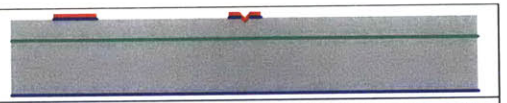
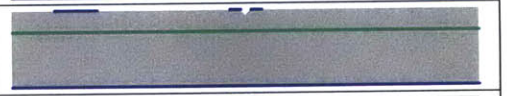
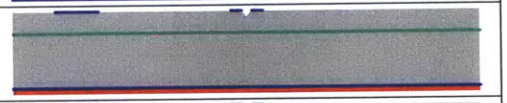
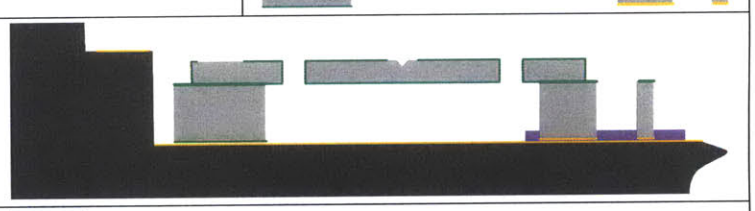
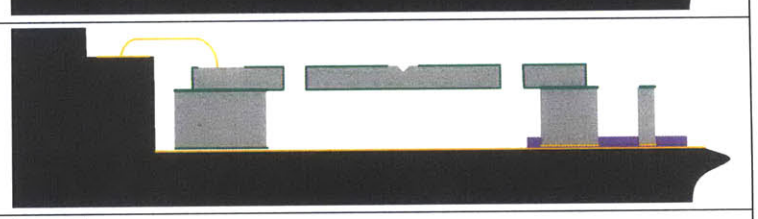
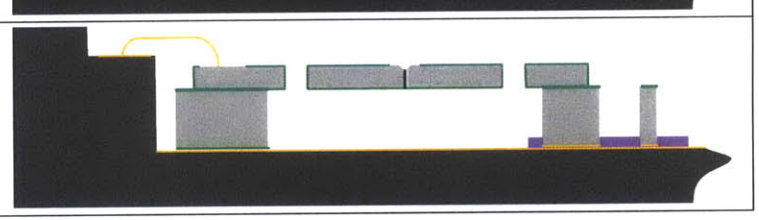
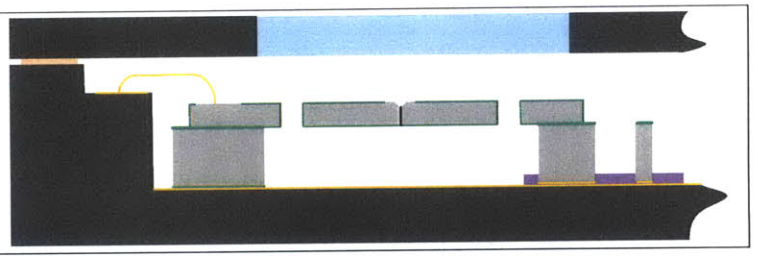
	Meta Description	Description	Lab	Machine	Recipe	
1	Wafers	Virgin 100 mm DSP SOI wafer, 10-20 μm device layer, 300 μm handle				
2	Deposit Nitride	RCA	ICL	RCA		
3		LPCVD Nitride		6D-nitride	150 nm	
4	Pattern Nitride I	HMDS	TRL	HMDS		
5		Deposit PR		coater	OCG-825	
6		Prebake		prebakeovn	30 minutes, 90°C	
7		Expose		EV-1	2 seconds	
8		Develop		photo-wet	OCG 934 1:1 1 min	
9		Postbake		postbake	30 minutes, 120°C	
10		Etch Nitride		AME5000	Chamber A: NITRIDE CF4, 66 seconds for 150 nm	
11		Strip Photoresist		acidhood2	piranha	
12	KOH Etch and Clean	KOH Etch	ICL	TMAH-KOHhood	5 minutes	
13		Yellow Piranha	TRL	Acidhood	Yellow, 10 min	
14		Green Piranha		Acidhood	Green, 10 min	
15		HF Dip		Acidhood	50:1, 15 seconds	
16	Pattern Nitride II	HMDS	TRL	HMDS		
17		Deposit PR		coater	OCG-825	
18		Prebake		prebakeovn	30 minutes, 90°C	
19		Expose		EV-1	2 seconds	
20		Develop		photo-wet	OCG 934 1:1 1 min	
21		Postbake		postbake	30 minutes, 120°C	

22		Nitride Etch		AME5000	Chamber A: NITRIDE CH4, 66 seconds for 150 nm	
23		Strip Photoresist		Acidhood2	piranha	
24	Handle Layer Etch	HMDS	TRL	HMDS		
25		Deposit PR		coater	AZ-4620	
26		Prebake		prebakeovn	60 minutes, 90°C	
27		Expose		EV-1	22 seconds	
28		Develop		photo-wet	AZ-440, 2 min	
29		Postbake		postbake	30 minutes, 90°C	
30		Etch Handle Layer		STS-1	NITRIDE for 4-5 min then MIT59	
31		Etch Buried Oxide		acidhood2	ultrasonic BOE, 15 minutes	
32		Strip Photoresist		acidhood2	piranha	
	Fabrication completed through step 32 before STS-1 became gold contaminated on September 29, 2004					
33	Nitride Strip	Hot Phosphoric Acid	ICL	nitrEtch-HotPhos	35 minutes, 4.5 nm/minute	
34	Nitride Deposition	Special VTR clean for post STS wafers	TRL	acidhood2	piranha	
35				asherTRL	1 hour	
36				acidhood2	piranha	
37				rcaTRL		
38		Deposit Nitride	ICL	VTR	150 nm	
39	Etch Handle Side Nitride		ICL	AME5000	Chamber A: NITRIDE CH4, 66 seconds for 150 nm patterned w/	

					shadow mask (see note 1)	
40	Etch Device Side Nitride	HMDS	TRL	HMDS		
41		Deposit PR		coater	OCG-825	
42		Prebake		prebakeovn	30 minutes, 90°C	
43		Expose		EV-1	2 seconds	
44		Develop		photo-wet	OCG 934 1:1 1 min	
45		Postbake		postbake	30 minutes, 120°C	
46		Etch Nitride	ICL	AME5000	Chamber A: NITRIDE CH4, 66 seconds for 150 nm	
47		Strip PR	TRL	Acidhood2	piranha	
48	Device Layer Etch	HMDS	TRL	HMDS		
49		Deposit PR		coater	OCG-825 double coat	
50		Prebake		prebakeovn	30 minutes, 90°C	
51		Expose		EV-1	22 seconds	
52		Develop		photo-wet	OCG 934 1:1	
53		Postbake		postbake	30 minutes, 120°C	
54		Etch Device Layer		STS-2	STShall, wafer mounted on handle	
55		Strip Photoresist		acidhood2	piranha	
57	Grow Oxide	RCA	TRL	rca-TRL	blow dry with air gun and then put empty cassette in the SRD	
58		Grow Oxide		A2-WetOxBond	300 nm of oxide, Recipe #5, 45 minutes of wet oxidation	
59	Expose Contacts	Remove Oxy-Nitride		acidhood2	BOE:DI Water 1:1 for 70 seconds, 65	

					nm/min – remove 750 A of oxide	
60		Strip Nitride	ICL	nitrEtch-HotPhos	35 minutes, 4.5 nm/minute	
61	Handle Layer Contacts	Deposit gold	TRL	e-beam	20 nm of titanium, 300 nm of gold, deposited through a shadow mask	
62	Dice Wafer	Break tabs with wafer mounted on porous aluminum vacuum chuck or cut the tabs by laser machining				
63	Assemble	Package is Kyocera PN: KD-78382-G-1 or NTK IDK24F1-167MAL. Adhesive is JMI 7000. Golden Altos of Milpitas CA does assembly, wirebonding, and sealing.				
64	Wirebond	Aluminum or gold wire, see wiring diagram (8 bonds)				
65	Fracture	Done with external probe				

66	Seal	HRC-372-21-50MT/100 GKL, Mil-Std-883, Method 1018 or Mil-Std-883, Method 5005, Table IV, Group D6 test	

Notes:

1. Use of shadow mask in AME5000 has been approved by Eric Lim. He will be present for the etch. Shadow mask will be fabricated using standard lithography and STS-2 in accordance with a previously approved process.
2. Shadow masks will be made from silicon wafers by DRIE in accordance with a previously approved process.

Change Log

January 17, 2005	Process created by modifying Fracturecap Rework Process.
February 15, 2005	After discussion with Professor Hoyt, process is approved.
April 28, 2005	Double coating during device layer etch

After concluding that oxide blunting was not damaging the KOH notches, and reasoning that thermally driven surface diffusion was the most likely culprit, this process (from Section 5.6) was designed to sidestep the problem of protecting the notches during high–temperature steps by etching the notches near the end of the process. To that end, a nitride diffusion barrier at the future site of the notch is used to create a hole in the thermal oxide grown after the device layer DRIE. After the nitride is stripped, the wafer is KOH etched with the thermal oxide as a mask.

Variable Capacitor Fabrication Process 3.0

This process is designed to produce variable capacitors from virgin SOI's

Alex Sprunt
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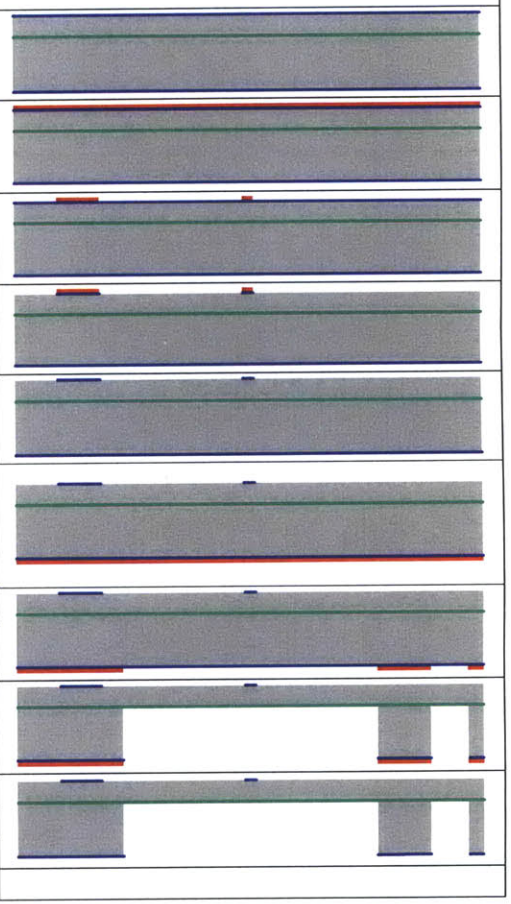
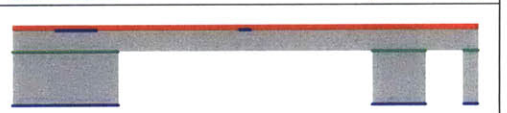
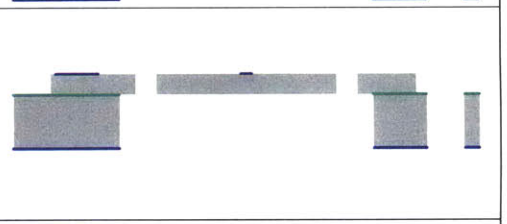
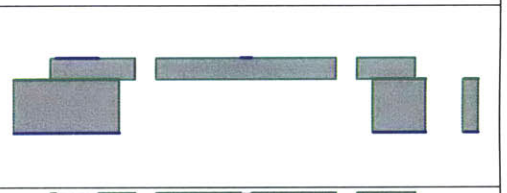
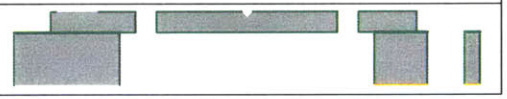
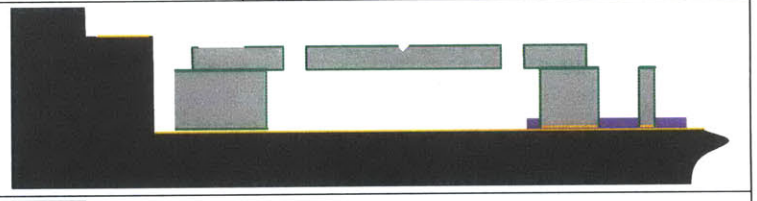
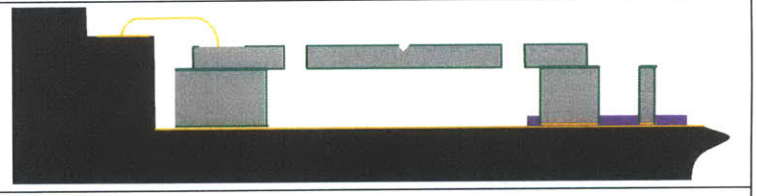
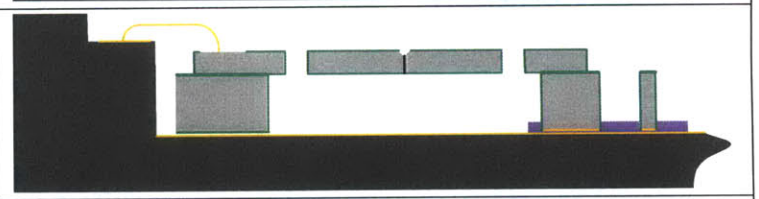
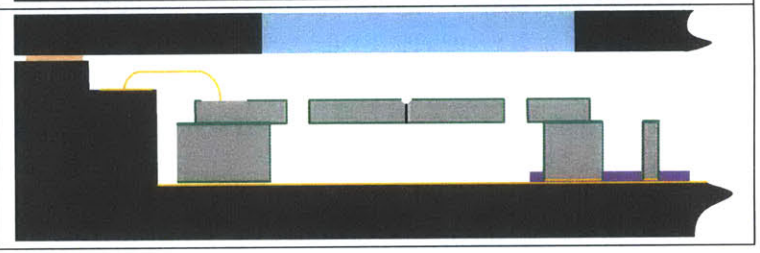
Room 3-470, x3-1953

	Meta Description	Description	Lab	Machine	Recipe
1	Wafers	Virgin 100 mm DSP SOI wafer, 10-20 μm device layer, 300 μm handle			
2	Deposit Nitride	Low Stress Nitride	ICL	VTR	150 nm
3	Pattern Device Side Nitride	HMDS	TRL	HMDS	
4		Deposit PR		coater	OCG-825
5		Prebake		prebakeovn	30 minutes, 90°C
6		Expose		EV-1	2.3 seconds
7		Develop		photo-wet	OCG 934 1:1 1 min
8		Postbake		postbake	30 minutes, 120°C
9		Etch Nitride	ICL	AME5000	Chamber A: NITRIDE CF4, 66 seconds for 150 nm
10		Strip Photoresist	TRL	acidhood2	piranha
11	Pattern Handle Layer	HMDS	TRL	HMDS	
12		Deposit PR		coater	AZ-4620 (double coat)
13		Prebake		prebakeovn	60 minutes, 90°C
14		Expose		EV-1	22 seconds
15		Develop		photo-wet	AZ-440, 3 min
16		Postbake		postbake	30 minutes, 90°C
17		Etch Handle Layer		STS-2	MIT59, switching to OLE3 when buried oxide appears
18		Dismount		Solvent-noAu	acetone dismount
19		Strip Photoresist		acidhood2	piranha
20				asher-TRL	30 minutes
21		Etch buried oxide		acidhood2	BOE, 15 minutes



22	Device Layer Etch	HMDS	TRL	HMDS		
23		Deposit PR		coater	OCG 825 (double coat)	
24		Prebake		prebakeovn	60 minutes, 90°C	
25		Expose		EV-1	6 seconds	
26		Develop		photo-wet	OCG 934 1:1 1 min	
27		Postbake		postbake	30 minutes, 90°C	
28		Etch Device Layer		STS-2	STShall, wafer mounted on handle	
29		Dismount		Solvent-noAu	acetone dismount	
30		Strip Photoresist		acidhood2	piranha	
31				asher-TRL	30 minutes	
32	Thermal Oxidation	RCA	TRL	rca-TRL	blow dry with air gun and then put empty cassette in the SRD	
33		Grow Oxide		A2-WetOxBond	300 nm of oxide, Recipe 5	
34	Open Oxide	Remove Oxy-Nitride	TRL	acidhood2	BOE:DI Water 1:1 for 70 seconds, ~30 nm/min – remove 750 A of oxide	
35		Strip Nitride	ICL	nitrEtch-HotPhos	60 minutes	
36	KOH Etch and Clean	KOH Etch	ICL	TMAH-KOHhood	20 minutes	
37		Yellow Piranha	TRL	Acidhood	Yellow, 10 min	
38		Green Piranha		Acidhood	Green, 10 min	
39		HF Dip		Acidhood	50:1, 15 seconds	
40	Handle Layer Contacts	Deposit gold		e-beam-Au	20 nm of titanium, 300 nm of gold, deposited through	

					a shadow mask	
41	Dice Wafer	Break tabs with wafer mounted on porous aluminum vacuum chuck or cut the tabs by laser machining				
42	Assemble	Package is Kyocera PN: KD-78382-G-1 or NTK IDK24F1-167MAL. Adhesive is JMI 7000. Golden Altos of Milpitas CA does assembly, wirebonding, and sealing.				
43	Wirebond	Aluminum or gold wire, see wiring diagram (8 bonds)				
44	Fracture	Done with external probe, followed by examination in SEM to check fracture surfaces.				
45	Seal	HRC-372-21-50MT/100 GKL, Mil-Std-883, Method 1018 or Mil-Std-883, Method 5005, Table IV, Group D6 test				

Notes:

1. Double coating with OCG 825 has been tested with 3 um features. Follow procedure in Appendix
2. For the handle layer etch, OLE3 is used once buried oxide appears because it has a better silicon to silicon oxide selectivity ratio, so is less likely to damage the oxide.
3. For good electrical contact during wirebonding, the device layer must be highly doped (5-18 mΩ-cm) p-type. Improperly doped wafers will form a schottky diode with the wirebond, precluding measurement of the fracture surfaces' capacitance.
4. Follow the procedure in the Appendix for mounting the wafers on handles. Handles are necessary for using the AME5000 and the STS-2. Acetone dismounting is gentler than dismounting in piranha.
5. Spinning resist onto the wafer after the handle layer DRIE is extremely difficult. The chief difficulty is with mounting the wafer on the spin coater in TRL. The best method found so far is to cover the coater's vacuum chuck with die-saw tape, trim the edges off the tape, and then slit the tape above a few of the vacuum channels.
6. After the device layer DRIE, wet wafers should be immersed in methanol, which should then be allowed to evaporate (in the fume hood). This is considerably easier and less risky than blowing the wafers dry with the nitrogen gun. The main exceptions are the dry following RCA, which should absolutely not be done with the SRD, the dry following the hot phosphoric acid etch, and the dry following the KOH etch. At those times, gently use the nitrogen gun; methanol drying is either unacceptable from a contamination point of view or impractical because no fume hood is available.
7. The nitride strip is of a generous length to ensure the nitride is fully stripped. Finding out a thin film of nitride is still present at the KOH hood is irritating.
8. The KOH etch is long to ensure the stress concentrating notches self-terminate with sharp roots.
9. The post-KOH clean is a good idea as a pre-wirebond clean, even if no metal deposition is done.
10. Metal deposition is necessary only if the die is to be assembled into the die cavity with JM7000 or some other adhesive. For eutectic bonding, no metallization is necessary and instruct Golden Altos to use the low temperature (300°C) process. Metal deposition has not been tested.

Change Log

April 7, 2005	Process created by modifying Fracturecap Process.
April 11, 2005	Process approved after addition of post-KOH clean
June 30, 2005	Added documentation of acetone dismounting and ashing, as well as some additional notes.

A.7 OCG 825 20CS Photoresist

Process parameters for coating wafers with OCG 825 20CS photoresist

HMDS	28 min approximately	recipe 5
Dispense	6 seconds	500 RPM[1]
Spread	6 seconds	750 RPM
Spin	30 seconds	2000 RPM
Pre-bake	30 minutes	90°C
Expose	2.3 seconds	
Develop	1 minute or until clear	OCG 934 1:1
Post-bake	30 minutes	120°C

Table A.1: Single coating OCG 825 20CS

HMDS	28 min approximately	recipe 5
Dispense	6 seconds	500 RPM
Spread	6 seconds	750 RPM
Spin	30 seconds	2000 RPM
Intermediate Bake	2 minutes	95°C
Dispense	6 seconds	500 RPM
Spread	6 seconds	750 RPM
Spin	30 seconds	200 RPM
Pre-bake	25 minutes	95°C
Expose	6 seconds	
Develop	1 minute or until clear	OCG934 1:1
Post-bake	120°C	30 minutes

Table A.2: Double coating OCG 825 20CS

[1] 200 RPM on oxide films

A.8 AZ P4620 Photoresist

Process parameters for coating wafers with AZ4620 photoresist

Dispense	10 seconds	0 RPM
Spread	10 seconds	0 RPM
Spin	60 seconds	1750 RPM
Pre-bake	1 hour	95°C
Expose	22 seconds	
Develop	2 minutes or until clear	AZ 440 MIF
Post-bake	25 minutes	95°C

Table A.3: Single coating AZ P4620

Dispense	10 seconds	0 RPM
Spread	10 seconds	0 RPM
Spin	60 seconds	1750 RPM
Intermediate Bake	10 minutes	95°C
Dispense	10 seconds	0 RPM
Spread	10 seconds	0 RPM
Spin	60 seconds	1750 RPM
Pre-bake	60 minutes	95°C
Expose	65 seconds	
Develop	3 minutes or until clear	AZ 440 MIF
Post-bake	25 minutes	95°C

Table A.4: Double coating with AZ P4620

A.9 Wafer Mounting

Coat backside of device wafer with OCG-825-20-CS resist using the single coat recipe

Bake device wafer for 5 minutes at 95°C

Coat handle wafer with AZ-P4620 resist at 2200 RPM in dispense mode. Make "bull's eye" target mount pattern with acetone squeeze bottle.

Slit the target with an acetone soaked Q-tip. Three slits are typical.

Place the device wafer on the handle wafer use the cap end of a Sharpie marker to keep the device wafer from sliding and to gently press device wafer into handle wafer

Bake at 90°C for 25 minutes

Appendix B

Variable Capacitor Diagrams

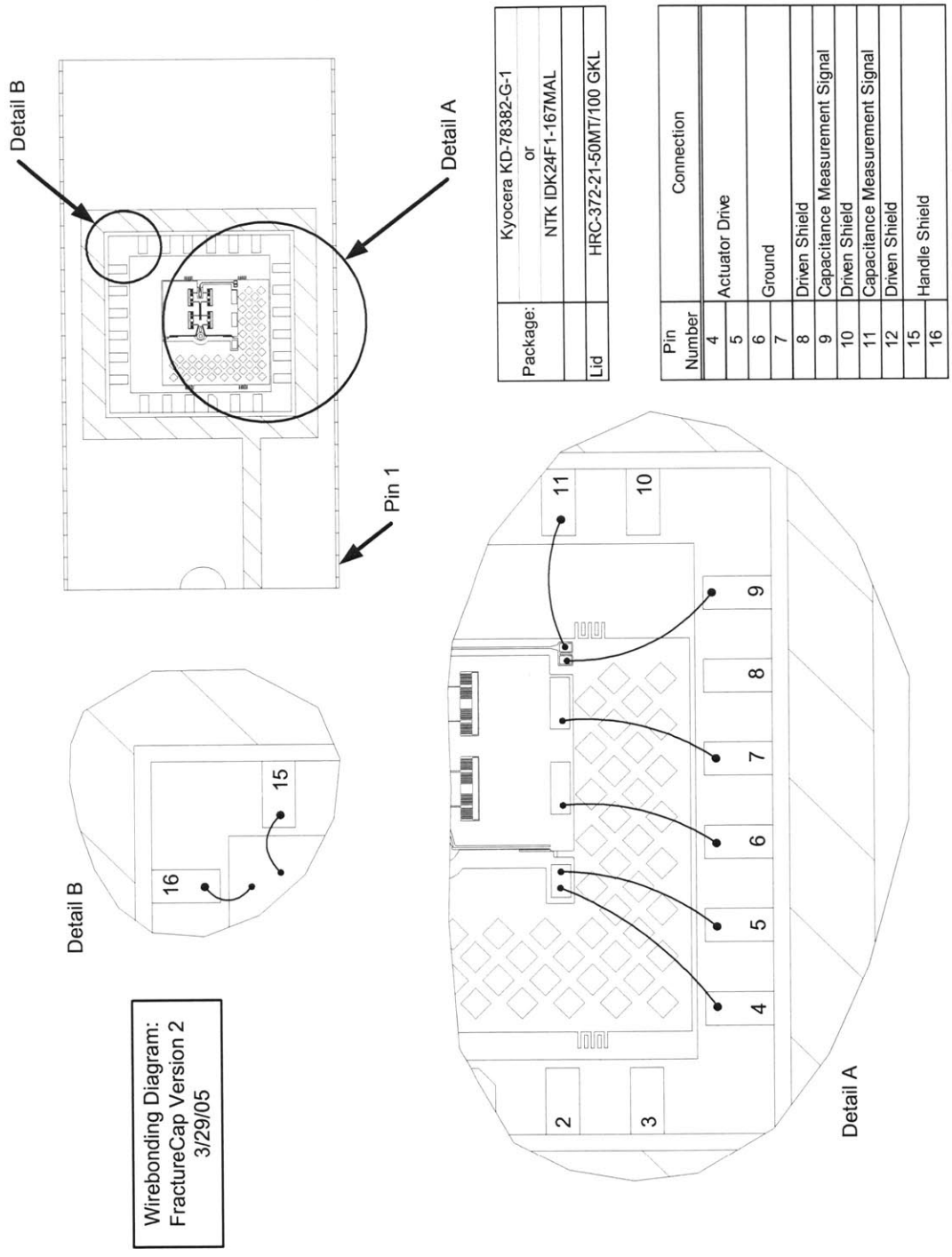
B.1 First Prototype Wire Bonding Diagram

Pin No.	Connection
1	Signal Shield 1
2	Signal
3	Signal Shield 2
4	Ground
5	
6	Actuator Drive
7	
15	Handle Shield
16	

Package is Kyocera
PN: KD-78382-G-1 or
Equivalent from NTK

Lid is HRC-372-21-50MT/100-GK

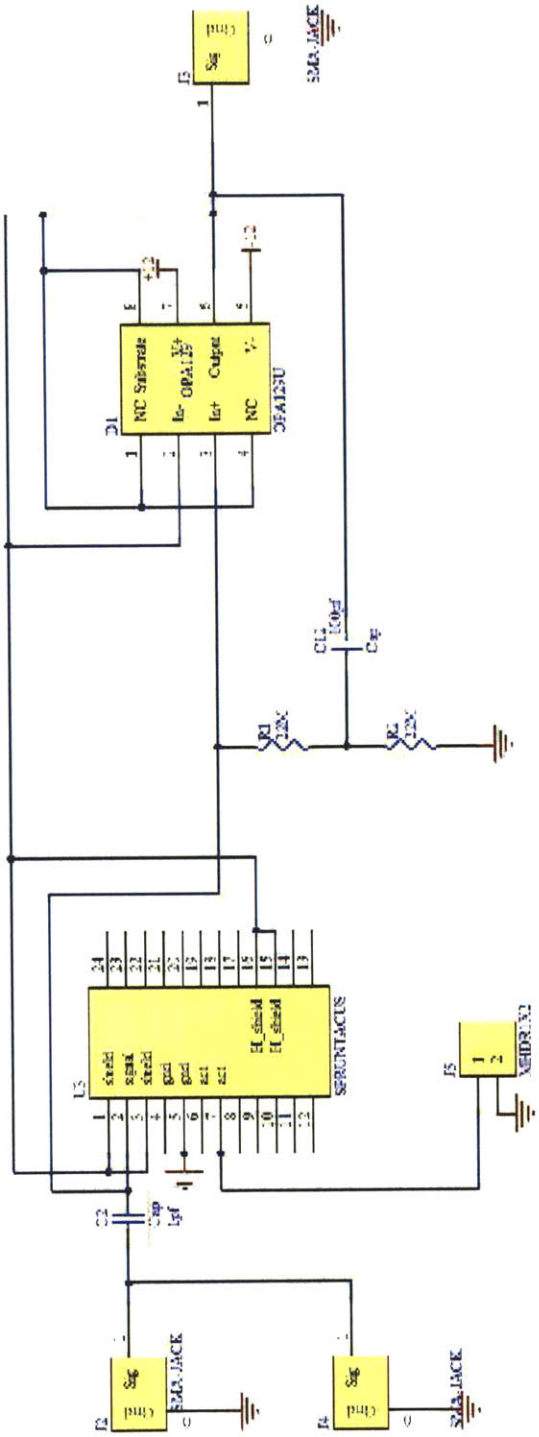
B.2 Second Prototype Wire Bonding Diagram



Package:	Kyocera KD-78382-G-1 or NTK IDK24F1-167MAL
Lid	HRC-372-21-50MT/100 GKL

Pin Number	Connection
4	Actuator Drive
5	
6	Ground
7	
8	Driven Shield
9	Capacitance Measurement Signal
10	Driven Shield
11	Capacitance Measurement Signal
12	Driven Shield
15	Handle Shield
16	

B.3 Capacitance Measurement Board Diagram



Appendix C

ANSYS Code

The code in this appendix constructs a portion of the geometry for the variable capacitor device and calculates the capacitance between the various different conductors. The output from the model supports the evaluation of the parasitics of the variable capacitor device (Section 4.1.4). The geometry is described parametrically to facilitate experimentation. A great deal of effort also went into the meshing; academic licences only support a limited number of nodes. The output from the program is a text file, "cmatrix.txt," giving the capacitance between the numbered conductors. The specimen anchor is conductor one, the flexure is conductor two, and the handle layer is conductor three.

```
/prep7

! All dimensions in microns

air_size=1000          ! Size of the air cube enclosing the device
device_depth=20        ! Thickness of the device layer
handle_depth=300       ! Thickness of the handle layer
displacement=1.5       ! Displacement of the ''flexure'' - controls
   gap opening
specimen_width=10      ! Width of the specimen
specimen_length=60     ! Length of the specimen
```

```
anchor_width=90      ! Width of the anchor region - minimum bond
    pad size is 100 um square
handle_tail=200      ! length of the "tail" for the handle layer
    extending beyond the anchor
gap=75               ! the space between the anchor region and the
     flexure frame
frame_length=520     ! length of the flexure frame
frame_width=750      ! overall width of the flexure frame
KOH_cut_width=3      ! width of KOH cut
oxide_depth=1.5      ! thickness of the oxide


oxide_permittivity=3.8  ! relative permittivity of the silicon
    oxide

! The value calculated for Cap13 should correspond well to the ''
    Mutual Capacitance between conductors  1. and  3.'' as given
    by the results window. This portion of the model can be
    approximated effectively by the parallel plate capacitor
    formula.

Cap13=oxide_permittivity*8.854e-6*0.5*(frame_length-
    specimen_length)*anchor_width/oxide_depth

et,1,123                    ! E-field Tetrahedron 123
et,2,122                    ! Brick 122, same as 123, but a
    brick
emunit,epzro,8.8            ! Set epsilon_0 to a value
    compatible with um (pF/m)
mp,perx,1,1                 ! Make the dielectric constant of
     air 1
```

```
mp, perx ,2 , oxide_permittivity      ! dielectric constant of silicon
    oxide.

wplane, ,0 ,0 , - device_depth/2      ! move the working plane down to
    make the device layer geometry

! Create the flexure frame
K,1 ,0 , displacement +0.5* frame_length , -0.5* device_depth
K,2 ,0.5* frame_width , displacement +0.5* frame_length , -0.5*
    device_depth
K,3 ,0.5* frame_width , displacement -0.5* frame_length , -0.5*
    device_depth
K,4 ,0.5* anchor_width+gap , displacement -0.5* frame_length , -0.5*
    device_depth
K,5 ,0.5* anchor_width+gap , displacement +0.5* specimen_length , -0.5*
    device_depth
K,6 ,0.5*( specimen_width+specimen_length ) , displacement +0.5*
    specimen_length , -0.5* device_depth
K,7 ,0.5* specimen_width , displacement , -0.5* device_depth
K,8 ,0 , displacement , -0.5* device_depth

! Make an area of the flexure frame keypoints
asel , none
A,1 ,2 ,3 ,4 ,5 ,6 ,7 ,8

! Create the Anchor
K,11 ,0 ,0 , -0.5* device_depth
K,12 ,0.5* specimen_width ,0 , -0.5* device_depth
K,13 ,0.5*( specimen_width+specimen_length ) , -0.5* specimen_length
    , -0.5* device_depth
K,14 ,0.5* anchor_width , -0.5* specimen_length , -0.5* device_depth
K,15 ,0.5* anchor_width , -0.5* frame_length , -0.5* device_depth
```

```
K,16,0,-0.5*frame_length,-0.5*device_depth
K,17,0,-0.5*specimen_length,-0.5*device_depth

! Make an area of the anchorside specimen keypoints
A,11,12,13,17
asel,none

! Make an area of the anchor underside (the buried oxide side)
A,17,14,15,16
cm,anchor_oxide_area,area

! extrude the areas to create volumes
asel,all
vext,all,,,0,0,device_depth

! Move and rotate the working plane to do KOH cuts
wplane,,0,0,device_depth/2
wprota,0,0,90

! Keypoints to create area for KOH cut on the flexure side of the
    capacitor
K,110,0,displacement,0.5*device_depth-0.5*KOH_cut_width*tan
   (54.7*3.14/180)
K,111,0,displacement+0.5*KOH_cut_width,0.5*device_depth
K,112,0,displacement,0.5*device_depth

! Make an area from the keypoints
asel,none
A,110,111,112

vext,all,,,3*specimen_width ! Extrude the area
```

```
vsbv,1,4,,delete,delete ! subtract the volumes from each other

! Keypoints to create area for KOH cut on the anchor side of the
    capacitor
K,113,0,0,0.5*device_depth-0.5*KOH_cut_width*tan(54.7*3.14/180)
K,114,0,0,0.5*device_depth
K,115,0,-0.5*KOH_cut_width,0.5*device_depth

! Make an area from the keypoints and extrude into a volume
asel,none
A,113,114,115
vext,all,,,3*specimen_width

vsbv,2,1,,delete,delete      ! subtract the volume from the anchor

wprota,0,0,-90               ! rotate the working plane back into
    position

wplane,,0,0,-device_depth/2 ! move the working plane to the
    bottom of the device layer

cmsel,s,anchor_oxide_area,area  ! select the bottom of the
    specimen anchor (where the oxide is)

vext,all,,,,,-oxide_depth       ! extrude that area to create the
     oxide volume

asel,s,loc,z,-1*(oxide_depth+0.5*device_depth)  ! select the
    bottom of that volume

vext,all,,,,,-handle_depth      ! extrude that out to create the
    handle layer
```

```
! Select the back of the handle layer volume
asel,s,loc,y,-0.5*frame_length
asel,r,loc,z,-1*(oxide_depth+0.5*device_depth+handle_depth),-1*(
    oxide_depth+0.5*device_depth)
vext,all,,,,-handle_tail          ! extrude that out to create the
    ''handle layer tail''
vsel,s,loc,z,-1*(oxide_depth+0.5*device_depth+handle_depth),-1*(
    oxide_depth+0.5*device_depth)
vadd,all                          ! combine the various handle
    layer volumes

wplane,,0,0,-0.5*air_size         ! move the working plane down to
    the bottom of the air cube

rectng,0,0.5*air_size,0.5*air_size,-0.75*air_size    ! make the
    air cube

asel,s,loc,z,-0.5*air_size        ! select the air cube bottom
cm,air_a,area                     ! and make it into a component

vext,all,,,0,0,air_size           ! make the area of the air cube a
     volume

cmdele,anchor_oxide_area          ! delete the component -> this
    prevents an error message after the vovlap,all

! subtract the device geometry from the aircube
vsel,all
vovlap,all
```

```
cmsel,s,air_a,area                    ! Make the bottom air area into a
    component
vsla,s                                ! select the area associated with
    the volume
/trlcy,volu,0.5,all                   ! turn the air translucent
cm,surrounding_air,volu               ! make the air volume a component

wplane,,0,0,0                         ! move the working plane back to
   the origin

nummrg,all                            ! merge all the nodes to prevent
   the formation of elements at volume boundaries
numcmp,node                           ! compress the node numbers

vsel,s,loc,z,-0.5*device_depth-oxide_depth,-0.5*device_depth     !
    select the oxide volume
cm,oxide_anchor,volu                  ! create a component
vatt,2,,2,                            ! set element type and material
   type to 2
esize,20*oxide_depth                  ! set the esize
mshape,0,3D                           ! mesh with bricks in 3D
mshkey,1                              ! mapped mesh
vsweep,all                            ! use sweeping (unclear why vmesh
    won't work)

cmsel,s,surrounding_air,volu          ! select the air
vatt,1,,1                             ! use element type and material
   type 1
smrt,8                                ! smartsize 8
mshkey,0                              ! free mesh
mshape,1,3D                           ! tetrahedrons for 3D meshing
vmesh,all                             ! mesh the damn thing
```

```
vsel,s,volu,,4                    ! select the anchor side of the
    gate
vsel,a,volu,,8
cm,anchor,volu                    ! make the volumes into a
    component
aslv,s                            ! select the associated areas
nsla,s,1                          ! group the nodes
cm,cond1,node                     ! and make them into a component

vsel,s,volu,,5                    ! select the flexure side of the
    gate
cm,flexure,volu
aslv,s                            ! select the associated areas
nsla,s,1                          ! group the nodes
cm,cond2,node                     ! and make them into a component

! select the handle layer volume
vsel,s,loc,z,-0.5*device_depth-oxide_depth-handle_depth,-0.5*
    device_depth-oxide_depth
cmsel,u,surrounding_air,volu
aslv,s                            ! select the associated areas
nsla,s,1                          ! select the associated nodes
cm,cond3,node                     ! create the third conductor

finish                            ! exit /prep7

/solu                             ! enter the solution part of the
    program

eqslv,jcg                         ! use the Jacobian solver - don't
    know why... Kate's MEMS book recommends
```

```
cmatrix,2,'cond',3,1              ! run the macro to measure
    capacitance, with 2 conductors

finish

! Redraw the model...
/prep7
vsel,all
aslv,s
vplot
finish
/eof
/eof
```

Appendix D

Matlab Code

This appendix includes the essential code for doing some of the more elaborate calculations featured in the main body of the text.

D.1 Variable Capacitor

The section includes the code for implementing the two-node model of the variable capacitor device featured in Section 4.4. The solutions of the ninth order polynomial produced by that model are solved and post-processed by the code in the section below.

```
% A bare bones version of fracturecap for inclusion as an appendix

function [x1,x2,V]=barebones(n,h,d,k_sg,k_zg,k_t)

% n is the number of points in the zipper voltage vector
% h is the thickness of the zipper beam
% d is the stroke of the zipper
% k_sg, k_zg, and k_t are various spring constants

% All lengths are in micros (um)                                    10
% All forces are in milliNewtons (mN)
```

```
% Wafer Data
native_oxide_thickness=0.002; % 2nm (in um) native oxide thickness - Madou
device_layer_thickness=20;
handle_layer_thickness=300;
ratio_oxide_above_surface=0.56;

% Zipper Parameters
h0=0.25; % thickness of the silicon oxide dielectric
Q=2.72e-6; % Constant
epsilon_r=3.8; % dielectric constant of silicon oxide'

delta=d+h0/epsilon_r;

% Node mass properties
m1=1;
m2=1;

% Capacitor Parameters
KOH_notch_width=3;
Specimen_width=10;
Specimen_height=device_layer_thickness-0.5*KOH_notch_width*tan(54.7*pi/180);
Specimen_area=Specimen_width*Specimen_height;
epsilon_0=8.85e-12; % farad/m
Capacitor_voltage=1; % V this is the height of the sine wave applied - 0.5Vpeak-peak;
Capacitor_voltage_rms=Capacitor_voltage*sqrt(2)/2;

% Calculate the Constant for the capacitive force equation
B=1000*epsilon_0*Capacitor_voltage_rms^2*(Specimen_area*1e-12)/(2*(1e-6)^2);

% Solve the polynomial
V=linspace(1,200,n);
C=2*Q*device_layer_thickness*(h/h0)^(0.75)*V.^(1.5);

phi=k_sg + k_zg + (k_sg*k_zg)/k_t;
theta=(1 + k_zg/k_t)*B;
psi=1 + k_sg/k_t;
```

```
eta=B/k_t;
                                                                    50
% Solve the polynomials (one for each voltage)
for i=1:n
    poly=[-psi*phi^2;
        delta*phi^2;
        0;
        -(2*phi*theta*psi + phi^2*eta + C(i)^2);
        2*phi*theta*delta;
        0;
        -(theta^2*psi + 2*theta*phi*eta);
        delta*theta^2;                                              60
        0;
        -theta^2*eta];
    solution(1:9,i)=roots(poly);
    % Evaluate the solutions to look for evaluate numerical error
    solution_evaluated(1:9,i)=polyval(poly,solution(1:9,i));
end;

[row_max,col_max]=size(solution);

% Remove the complex solutions - they're non-physical               70
row_hold=9*ones(n,1);
tag=60; % the tag has got to be something, might as well be 60

for col=1:col_max
    for row=1:row_max
        if isreal(solution(row,col))==0
            solution(row,col)=tag; % used as a random tag
            row_hold(col)=row_hold(col)-1;
        end;
    end;                                                            80
end;

% Sort the solutions
solution=sort(solution,1);
```

```
% Remove the solutions that are entirely NaN
solution=solution(1:max(row_hold),:);

solution_gathered(:,n)=solution(:,n);

% Stitch the solutions together
for i=1:(n-1)
    seed=solution_gathered(:,n-i+1);
    feed=solution(:,n-i);
    solution_gathered(:,n-i)=link(feed,seed);
end;

[row_max,col_max]=size(solution_gathered);

for row=1:row_max
    for col=1:col_max
        if solution_gathered(row,col)==tag
            solution_gathered(row,col)=NaN;
        end;
    end;
end;

x1=solution_gathered;

% Remove the remaining aphysical solutions

% Remove all negative x1's:
% I am removing individual elements from the matrix here, but the effect seems to be
% the elimination of entier rows (solution sets) from x1. I have tested this out
% through n=100;
for row=1:row_max
    for col=1:col_max
        if x1(row,col)<0
            x1(row,col)=NaN;
        end;
```

```
    end;
end;

% now calculate x2
x2=x1*(1+k_sg/k_t) + B./(k_t*x1.^2); % Verified

% Remove all the values of x2 that exceed d, the maximum zipper displacement
index=1;
for row=1:row_max
    for col=1:col_max                                                    130
        if x2(row,col)>d
            x2(row,col)=NaN;
            x1(row,col)=NaN;
        end;
    end;
    % if a row is composed entirely of NaN's remove the row
    if min(isnan(x1(row,:)))==0
        x1_temp(index,:)=x1(row,:);
        x2_temp(index,:)=x2(row,:);
        index=index+1;                                                   140
    end;
end;

x1=x1_temp;
x2=x2_temp;

% Now would be a good time to eliminate the leading NaN's from x1 and x2
% All the NaN's in x2 come from x1, so I will only search in x1 and
% automatically remove them from x2.
                                                                         150
for col=1:col_max
    if min(isnan(x1_temp(:,col)))==0
        if max(isnan(x1_temp(:,col)))==1
            disp('Problem with removal of leading NaN''s. Column is not pure NaN');
        end;
        break;
```

```
    end;
end;

x1=x1_temp(:,col:length(x1_temp));
x2=x2_temp(:,col:length(x2_temp));

% Shorten the voltage and C vectors appropriately
V=V(:,col:length(V));
C=C(:,col:length(C));

[row_max,col_max]=size(x1);

% Stability Analysis

M=[m1 0;
    0 m2]; % Mass matrix

% Build the stiffness matrix (K) and calculate the squares of the
% linearized natural frequencies (lambda) for each of the stable
% and unstable solutions
for s=1:row_max % s sets which solution is being worked on
    for i=1:col_max % i moves through the solution

        K=[k_sg + k_t - (2*B)/(x1(s,i))^3 -k_t;
            -k_t (k_t + k_zg - C(i)/(2*(delta - x2(s,i))^(1.5)) )];
        % calculate the eigenvalues, equivalent to the square of
        % natural frequency
        raw_lambda(:,i)=eig(inv(M)*K);
    end;
    % interested only in the minimum eigenvalue, becuase the sign
    % of the minimum value determines stability; negative values
    % are unstable.
    lambda(s,:)=min(raw_lambda);
end;
```

D.1.1 Stitching the Solutions

The function in this section stitches together the solutions to the ninth order polynomial found in the previous section. The algorithm is not perfect, and could produce incorrect results, but it is sufficiently robust for this application.

```
function [out] = link(feed,seed)

feed_start=feed;
seed_start=seed;

% Puts the neighbors in the correct order, but
% scrambles the seed as well as the feed

for i=1:length(feed)                                    10
    [removed,feed,seed]=link_internal(feed,seed);
    keep(i,:)=removed;
end;

% Now the order of the seed must be restored with the feed values
% being moved as appropriate

for i=1:length(seed_start)
    target=seed_start(i);
    for j=1:length(seed_start)                          20
        if keep(j,2)==target
            final_feed(i)=keep(j,1);
        end;
    end;
end;

out=transpose(final_feed);

% Internal Function
function [removed,new_feed,new_seed] = link_internal(feed,seed)   30
```

```
seed_length=length(seed);
feed_length=length(feed);

% Build a pair of matrices to determine the distance between
% the different elements in the feed and seed
for i=1:seed_length
    feed_matrix(:,i)=feed;
end;

for i=1:feed_length
    seed_matrix(i,:)=seed';
end;

% This is that distance
difference=abs(feed_matrix-seed_matrix);

[a,b]=size(difference);

if a==1
    % This is a special case when either the feed is just a number
    % The following code picks which element of the seed is closest
    % to which element of the feed.
    row_min=1;
    [junk,col_min]=min(difference);
    feed_remove=1;
    seed_remove=col_min;
    new_feed=[];
else
    % Does the same as the loop above except for the more likely case
    % where the feed is a vector. One minimum operation determines which
    % element of the seed to work with, the other determines which element
    % of the feed.
    [d2,row_min]=min(difference);
    [junk,col_min]=min(d2);
    feed_remove=row_min(col_min);
```

```
    seed_remove=col_min;
    % Generate the new feed
    for i=1:feed_remove-1
        new_feed(i)=feed(i);
    end;
    for i=feed_remove:(length(feed)-1)
        new_feed(i)=feed(i+1);
    end;
    new_feed=new_feed';
end;

new_seed=[];

% Generate the new seed
for i=1:seed_remove-1
    new_seed(i,1)=seed(i,1);
end;

for i=seed_remove:(length(seed)-1)
    new_seed(i,1)=seed(i+1,1);
end;

% This is what's been taken out.
removed=[feed(feed_remove),seed(seed_remove)];
```

D.2 Capacitance Sensing Circuit

The code in this section uses the Matlab function "fmincon" to fita a model to experimental data to produce estimates for the values of capacitors C_2 and C_3 in the capacitance measurement circuit (Section 5.2.6).

```
function [X_nogradient] = fit(output);
% if output==1, it will print the figure to file

% This is the data gathered with the test capacitors he first column is the measured
```

```
% capacitance at 50 kHz using the LEES LCR meter.
% The second column is the output voltage (mV) of Hong Ma's board
data=[0.05 747;
    1.34 402;
    1.89 329;
    2.36 276;
    2.85 238];

Vo=data(:,2); % The voltage output data
C1_data=data(:,1); % The capacitance values data
Vin=980; % The input voltage (mV) 50kHz sine wave

% X=FMINCON(FUN,X0,A,B,Aeq,Beq,LB,UB,NONLCON);
x0=[0.8811 0]; % [C2 C3] - guesses for the values of C2 and C3
lb=[0 0]; % Setting the lower bound for each
ub=[2 2]; % Setting the upper bound
options=optimset('GradObj','on'); % Instructing fmincon to use the gradient option

% X=fmincon(at_costfun,x0,[],[],[],[],lb,ub,[],options,data,Vin);
X_nogradient=fmincon(@costfun,x0,[],[],[],[],lb,ub,[],[],data,Vin); % without gradient
X_gradient=fmincon(@costfun,x0,[],[],[],[],lb,ub,[],options,data,Vin); % with gradient

C1_model=linspace(0,3,100); % Some values for C1 to use for plotting

C2_fit=X_nogradient(1); % The values of the parameters for non-gradient
C3_fit=X_nogradient(2);

C2_fit_grad=X_gradient(1); % parameter values for gradient
C3_fit_grad=X_gradient(2);

% Build a figure to display the results
figure(1);
clf;
plot(data(:,1),data(:,2)/Vin,'go',...
    C1_model,circuit(Vin,C1_model,C2_fit_grad,C3_fit_grad)/Vin,'r-');
xlabel('Capacitance (pF)');
```

```
ylabel('Magnitude');
legend('Data','Fitted Model');

% Output the figure to file
if output==1
   exportfig(gcf,'c:\fracturegate\Figures\sensing-circuit-test.eps');
end;

% This function describes the output of the circuit in terms of the parameters
function [Vo] = circuit(Vin,C1,C2,C3)                                    50
Vo = Vin * ( C2 ./ (C1 + C2 + C3) );

% This function calculates the cost function and the gradient of the cost function
function [f,g] = costfun(x,data,Vin)
Vo=data(:,2); % Once again, pulling the output voltage from the data matrix
C1_data=data(:,1); % pulling the capacitance values from the data matrix
C2=x(1); % These are the unknown capacitor values being sought
C3=x(2);

f = sum((Vo - circuit(Vin,C1_data,C2,C3)).^2); % cost function           60

% Gradients with respect to C2 and C3
g(1) = sum( 2*(Vo - Vin*C2./(C1_data+C2+C3)).*-Vin.*(C1_data+C3)./((C1_data+C2+C3).^2));
g(2) = sum( 2*(Vo - Vin*C2./(C1_data+C2+C3)).*Vin.*C2./((C1_data+C2+C3).^2));
```

Appendix E

Anisotropic Material Properties of Single Crystal Silicon for FEA

Single crystal silicon is a anisotropic material. This appendix describes the conversion of silicon's anisotropic material properties from the forms in which they are available in the literature to a form compatible with Pro/Engineer. The proper material orientation with respect to the wafer is also explained.

E.1 Material Properties

Senturia [124] provides the properties in terms of the stiffness matrix, C, where the axes are aligned with the silicon's "natural coordinate system," the planes of its cubic structure (100), (010), and (001):

$$\begin{pmatrix} \sigma_x \\ \sigma_y \\ \sigma_z \\ \tau_{yz} \\ \tau_{zx} \\ \tau_{xy} \end{pmatrix} = \begin{pmatrix} c_{11} & c_{12} & c_{12} & 0 & 0 & 0 \\ c_{12} & c_{11} & c_{12} & 0 & 0 & 0 \\ c_{12} & c_{12} & c_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & c_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & c_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & c_{44} \end{pmatrix} \begin{pmatrix} \epsilon_x \\ \epsilon_y \\ \epsilon_z \\ \gamma_{yz} \\ \gamma_{zx} \\ \gamma_{xy} \end{pmatrix} \tag{E.1}$$

where

$$\begin{aligned} c_{11} &= 166 \quad GPa \\ c_{12} &= \ 64 \quad GPa \\ c_{44} &= \ 80 \quad GPa \end{aligned} \tag{E.2}$$

The compliance matrix, S, is the inverse of the stiffness matrix:

$$\boldsymbol{\sigma} = \boldsymbol{C\epsilon} \tag{E.3}$$

$$\boldsymbol{\epsilon} = \boldsymbol{S\sigma} \tag{E.4}$$

$$\boldsymbol{S} = \boldsymbol{C}^{-1} \tag{E.5}$$

It is not an error that the stiffness matrix is denoted C and the compliance matrix is denoted S; this confusing choice of nomenclature pervades the literature.

Brantley [16] provides values for silicon's stiffness (which match up with Senturia's) as well as values for silicon's compliance:

$$\begin{aligned} s_{11} &= \ \ 0.00768 \quad GPa^{-1} \\ s_{12} &= -0.00214 \quad GPa^{-1} \\ s_{44} &= \ \ 0.0126 \quad GPa^{-1} \end{aligned} \ . \tag{E.6}$$

A quick excursion to Matlab will verify Equation E.5 and that the compliance values in Equation E.6 are compatible with the stiffness values in Equation E.2.

Pro/Engineer [111] uses Tsai's definition [137] of poisson's ratio:

$$\begin{pmatrix} \epsilon_{11} \\ \epsilon_{22} \\ \epsilon_{33} \\ 2\epsilon_{12} \\ 2\epsilon_{13} \\ 2\epsilon_{23} \end{pmatrix} = \begin{pmatrix} \frac{1}{E_1} & \frac{-\nu_{12}}{E_2} & \frac{-\nu_{13}}{E_3} & 0 & 0 & 0 \\ \frac{-\nu_{21}}{E_1} & \frac{1}{E_2} & \frac{-\nu_{23}}{E_3} & 0 & 0 & 0 \\ \frac{-\nu_{31}}{E_1} & \frac{-\nu_{32}}{E_2} & \frac{1}{E_3} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{G_{21}} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{G_{31}} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{G_{32}} \end{pmatrix} \begin{pmatrix} \sigma_{11} \\ \sigma_{22} \\ \sigma_{33} \\ \sigma_{12} \\ \sigma_{13} \\ \sigma_{23} \end{pmatrix} \tag{E.7}$$

Although the indices are different on opposite sides of the diagonal, the matrix is symmetrical. Equation E.7 is in the form of a compliance, rather than a stiffness, matrix so Brantley's values for silicon's compliance will be the source for our inputs into Pro/Engineer. The use of $2\epsilon_{ij}$ instead of γ_{ij} is a notation issue only, $2\epsilon_{ij} = \gamma_{ij}$. It's also not significant that shear stresses and strains are in different orders in Equations E.7 and E.1; they may be re-ordered without distortion. For silicon it is particularly unimportant since all three shear moduli have the same value.

Pro/Engineer has three different material descriptions: isotropic, transverse isotropic, and orthotropic. These types of materials are described by two, five, and nine independent constants respectively. Silicon has three, so a transversely isotropic description would seem natural. Sadly, the stiffness matrix of a transversely isotropic material takes the following form [137]:

$$\boldsymbol{\sigma} = \begin{pmatrix} c_{11} & c_{12} & c_{12} & 0 & 0 & 0 \\ c_{12} & c_{22} & c_{23} & 0 & 0 & 0 \\ c_{12} & c_{23} & c_{22} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{c_{22}-c_{23}}{2} & 0 & 0 \\ 0 & 0 & 0 & 0 & c_{66} & 0 \\ 0 & 0 & 0 & 0 & 0 & c_{66} \end{pmatrix} \boldsymbol{\epsilon}, \tag{E.8}$$

which is incompatible with a description of silicon because its

$$\begin{aligned} C(4,4) &\neq \frac{C(2,2) - C(2,3)}{2} \\ c_{44} &\neq \frac{c_{11} - c_{12}}{2} \end{aligned} \tag{E.9}$$

That leaves the orthotropic description. The nine necessary constants are calculated from the three independent constants as follows:

$$
\begin{aligned}
E_1 &= \frac{1}{S(1,1)} = \frac{1}{s_{11}} = 130.132 \quad GPa \\
E_2 &= \frac{1}{S(2,2)} = \frac{1}{s_{11}} = 130.132 \quad GPa \\
E_3 &= \frac{1}{S(3,3)} = \frac{1}{s_{11}} = 130.132 \quad GPa \\
\nu_{21} &= \frac{-S(2,1)}{S(1,1)} = \frac{-s_{12}}{s_{11}} = 0.2783 \\
\nu_{31} &= \frac{-S(3,1)}{S(1,1)} = \frac{-s_{12}}{s_{11}} = 0.2783 \\
\nu_{32} &= \frac{-S(3,2)}{S(2,2)} = \frac{-s_{12}}{s_{11}} = 0.2783 \\
G_{21} &= \frac{1}{S(4,4)} = \frac{1}{s_{44}} = 79.560 \quad GPa \\
G_{31} &= \frac{1}{S(5,5)} = \frac{1}{s_{44}} = 79.560 \quad GPa \\
G_{32} &= \frac{1}{S(6,6)} = \frac{1}{s_{44}} = 79.560 \quad GPa
\end{aligned}
\tag{E.10}
$$

For an isotropic material, the typical inputs would be Young's modulus and Poisson's ratio. The shear modulus would be calculated from those two constants using the expression [35]:

$$
G = \frac{E}{2\,(1+\nu)}. \tag{E.11}
$$

Calculating the shear modulus of silicon from the values for Young's modulus and Poisson's ratio in Equation E.10 yields a value of 50.9 GPa, which is 36% less than the true value. Another measure of Silicon's anisotropy is its anisotropy ratio [45]:

$$
A.R. = \frac{2c_{44}}{c_{11} - c_{12}} = \frac{2\,(s_{11} - s_{12})}{s_{44}}. \tag{E.12}
$$

Silicon's value for which is 1.57, compared to a value of unity for a truly isotropic material.

E.2 Material Orientation

In addition to the material properties, a material orientation must be set. The wafer flat is oriented to the (110) plane and the wafer surface is typically (100) [33], so the material orientation is 45° off from the wafer flat (see Figure E-1). It is important to both create and assign the material orientation.

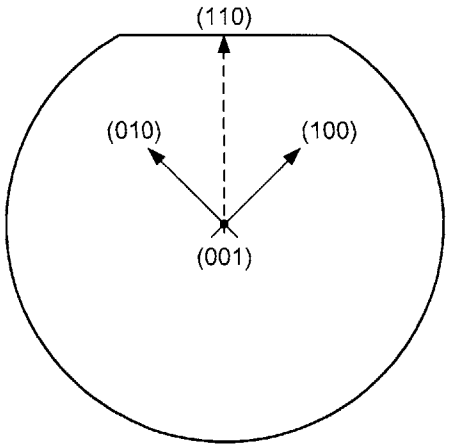


Figure E-1: Crystal structure orientation with respect to wafer.

E.3 Testing the Model

Brantley calculates Young's modulus for certain directions within important crystal planes. For the (100) plane, Young's modulus has a value of 168.9 GPa in the <011> direction and 130.2 GPa in the <001> direction. To test the material model, the part shown in Figure E-2 was built. The part consists of square sectioned rods, numbered one through three, at different orientations. The orientation of the part with respect to the silicon's crystal structure is denoted by a. Each rod is 1 m long and 0.05 m wide; the aspect ratio of 20:1 minimizes edge effects.

The rods are fully constrained in x, y, and z at their ends near the origin and then a displacement of 0.01 m is imposed (while simultaneously constraining motion perpendicular to the rod's axis). The force necessary to impose the displacement is then measured and used to calculate the Young's modulus of the rod:

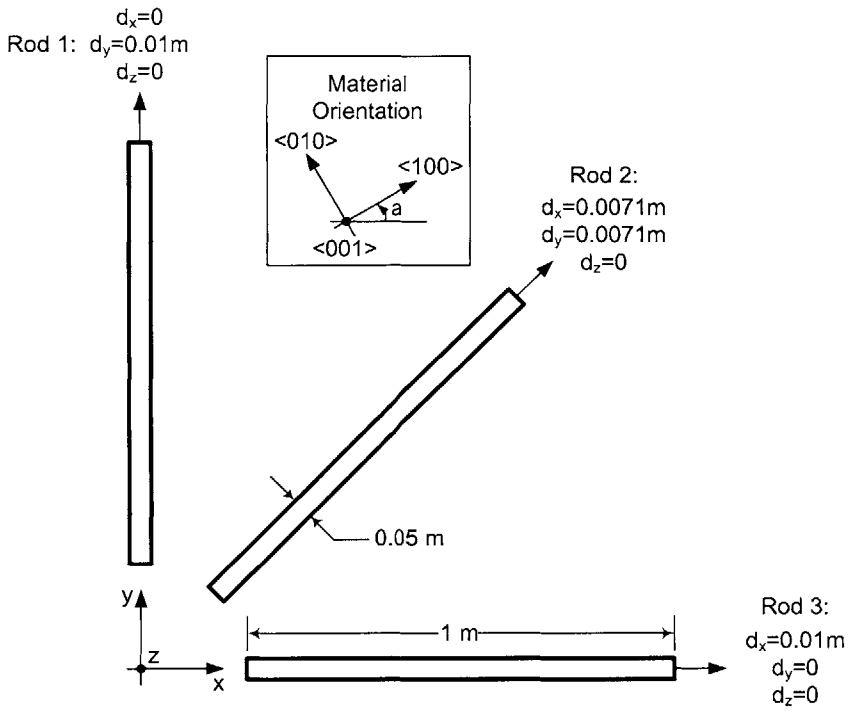


Figure E-2: Solid model with which to test the material properties model.

$$E = \frac{FL}{A\delta}, \tag{E.13}$$

where F, L, and A are the force, the rod length, and the rod's cross-sectional area respectively. This is not an ideal test, as the displacements imposed at both ends of the rods restrict its ability to contract, but given the limitations on the sorts of measurements Pro/E can make and the aspect ratio of the rods, the test is reasonable. The results of the test are in Tabel E.1. The anticipated values for Young's modulus agree quite well with the values derived from the model results, and as the Anisotropic II data shows, the model responds properly to a rotation of the crystal structure with respect to the part.

	Isotropic	Anisotropic I	Anisotropic II
Rotation, a	-	0	45°
$E_{1,anticipated}$ (GPa)	160	130.2	168.9
$E_{2,anticipated}$ (GPa)	160	168.9	130.2
$E_{3,anticipated}$ (GPa)	160	130.2	168.9
$Reaction_1$ (MN)	4.04	3.28	4.25
$Reaction_2$ (MN)	4.06	4.27	3.30
$Reaction_3$ (MN)	4.04	3.29	4.25
E_1 (GPa)	160	130	170
E_2 (GPa)	160	170	130
E_3 (GPa)	160	130	170

Table E.1: Summary of results from the test part. The model was run repeatedly to improve convergence, which was typically below 1%.

E.4 Isotropic Modelling of Silicon

Values of 160 GPa for Young's modulus and 0.25 for Poisson's ratio are frequently used in isotropic models for silicon. It's surprising that such a large value for Young's modulus is used; doing a angular average yields a considerably lower value [124]:

$$\left.\frac{1}{E}\right|_{average} \approx 0.6s_{11} + 0.4s_{12} + 0.25s_44 \Rightarrow E_{average} = 145\,GPa. \tag{E.14}$$

Simulations using the higher value (160 GPa) are successful because, deliberately or not, the designer has created a structure with stresses that are primarily in the <110> direction, i.e. perpendicular or parallel to the wafer's major flat. Designers simulating more complicated states of stress should be cautious using an isotropic model.

E.5 Notes

Senturia's book has an appendix describing the rotation of stiffness or compliance matrices to directions other than the principle axes (which is the orientation of the matrices given here). He references Nye [110] for a more complete discussion and the Handbook of Chemistry and Physics [83] for additional material properties.

Brantley's article also includes information on silicon's invariant planes and the stiffness and compliance of GaAs, GaP, and Ge.

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